

Page	Title of schematic page	Rev.	Date
01	Page List		
02	Block Diagram		
03	Change List		
04	BDW MCP(DISPLAY/Sideband)		
05	BDW MCP(MEMORY/GND)		
06	BDW MCP(CFG/PwrMGT)		
07	BDW MCP(POWER)		
08	BDW PCH(RTC/HDA/SATA)		
09	BDW PCH(PCIE/USB/Power M)		
10	BDW PCH(CLK/LPC/SPI/SMB)		
11	BDW PCH(GPIO/LPIO/MISC)		
12	BDW PCH(POWER)		
13	DDR3L MEMORY_x16(CH-A)		
14	DDR3L MEMORY_x16(CH-B)		
15	DDR3L TERMINATION		
16	HOLE/EMI/KB		
17	NPCE985L & FLASH		
18	eDP\TS\Camera		
19	To CARD READER BOARD		
20	HDMI/Thermal		
21	USB/USB repeater		
22	LAN RTL8111GS		
23	WLAN/KB-BL		
24	SSD/TP/FAN		
25	AUDIO(ALC233-CG)HP&MIC		
26	LED/PS/DMIC/TPM		
27	DP to VGA (PTN3355)		
28	Green Clock(SLG3NB3454)		
29	POWER +VCC_CORE (NCP81101)		
30	POWER 3.3V/5V-NB671L/NB670		
31	POWER 1.35VSUS/VTT_MEM		
32	POWER +1.05V /Thermal/+1.5V		
33	POWER CHARGER (ISL88732)		
34	POWER(BAT IN / ADA IN/ UL)		
35	IO PORT LIST		
36	Power Design Diagram		

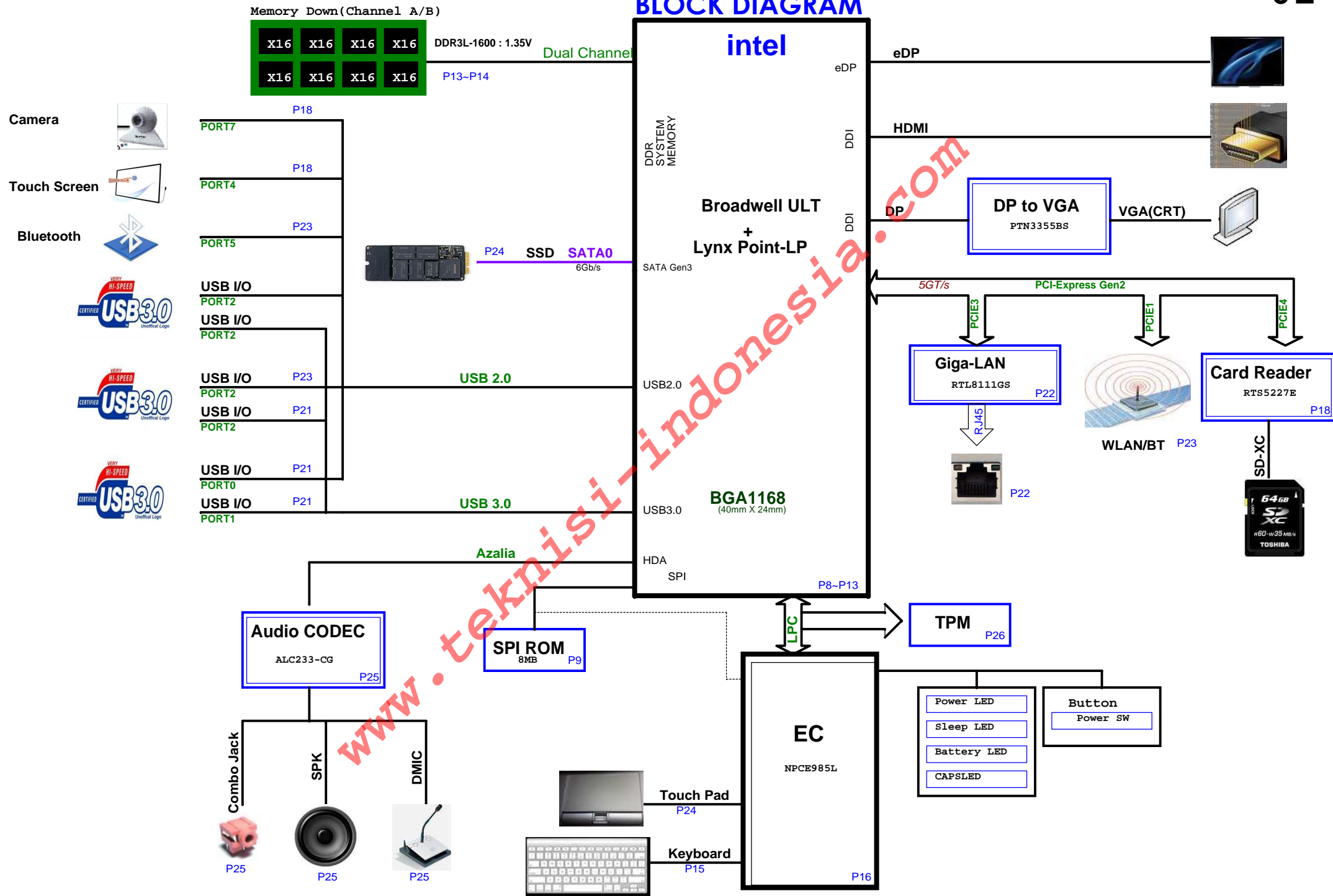
Page	Title of schematic page	Rev.	Date

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

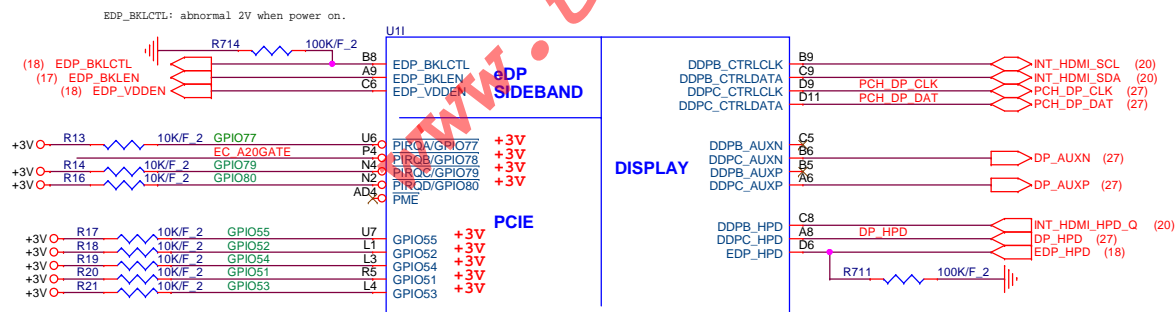
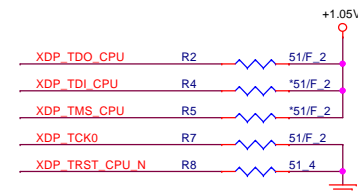
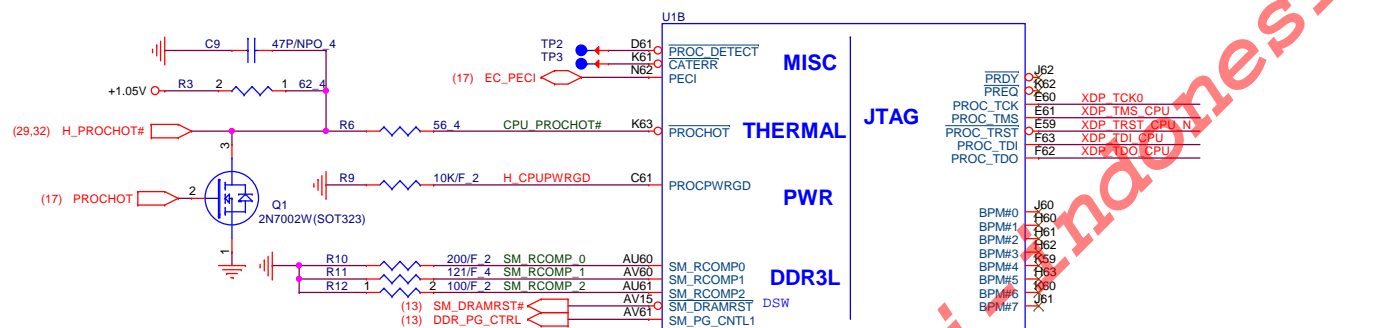
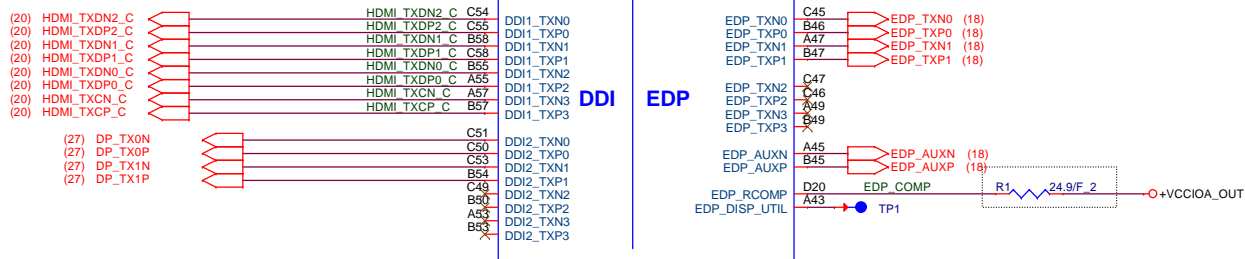
www.teknisi-indonesia.com

Broadwell ULT BLOCK DIAGRAM

02



INT. HDMI



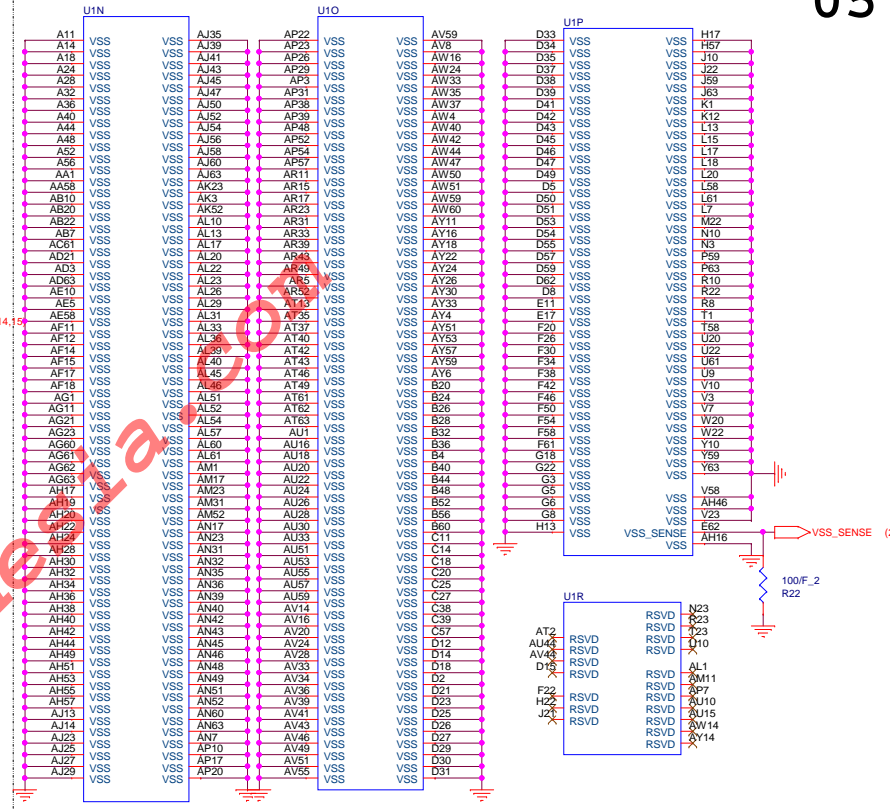
PTN3355B8 HPD pin had internal pull down 100K ohm, so that R712 can be reserved.

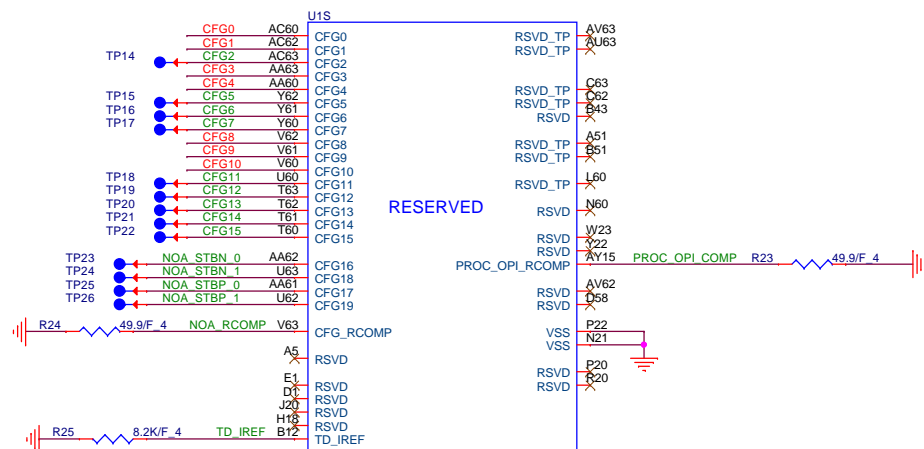


Quanta Computer Inc.

PROJECT : MS8

BDW MCP(Display/eDP)





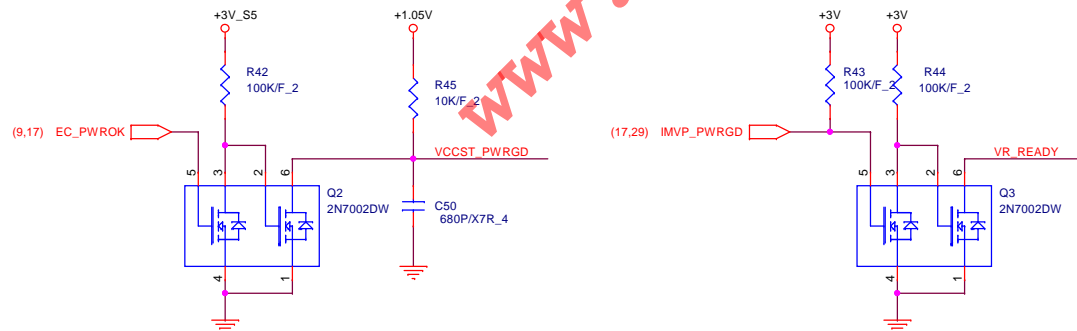
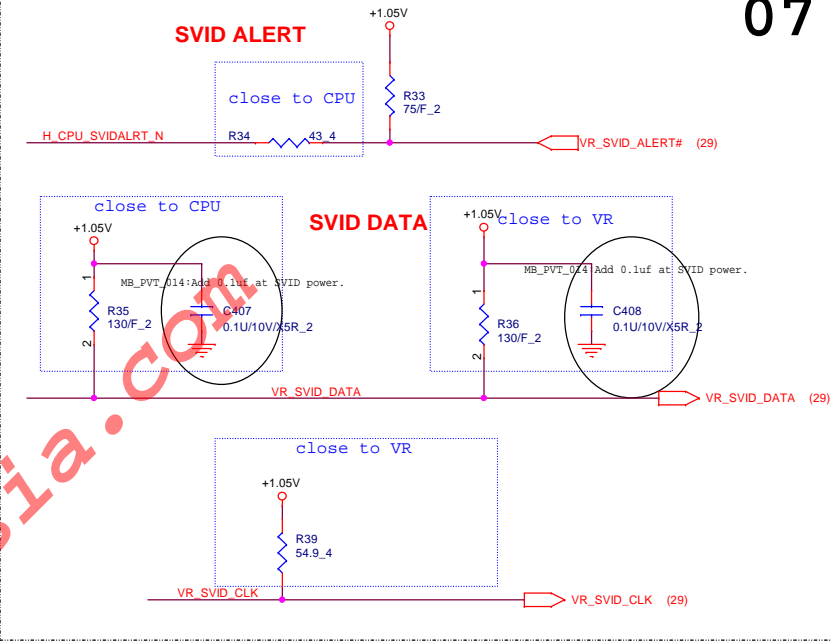
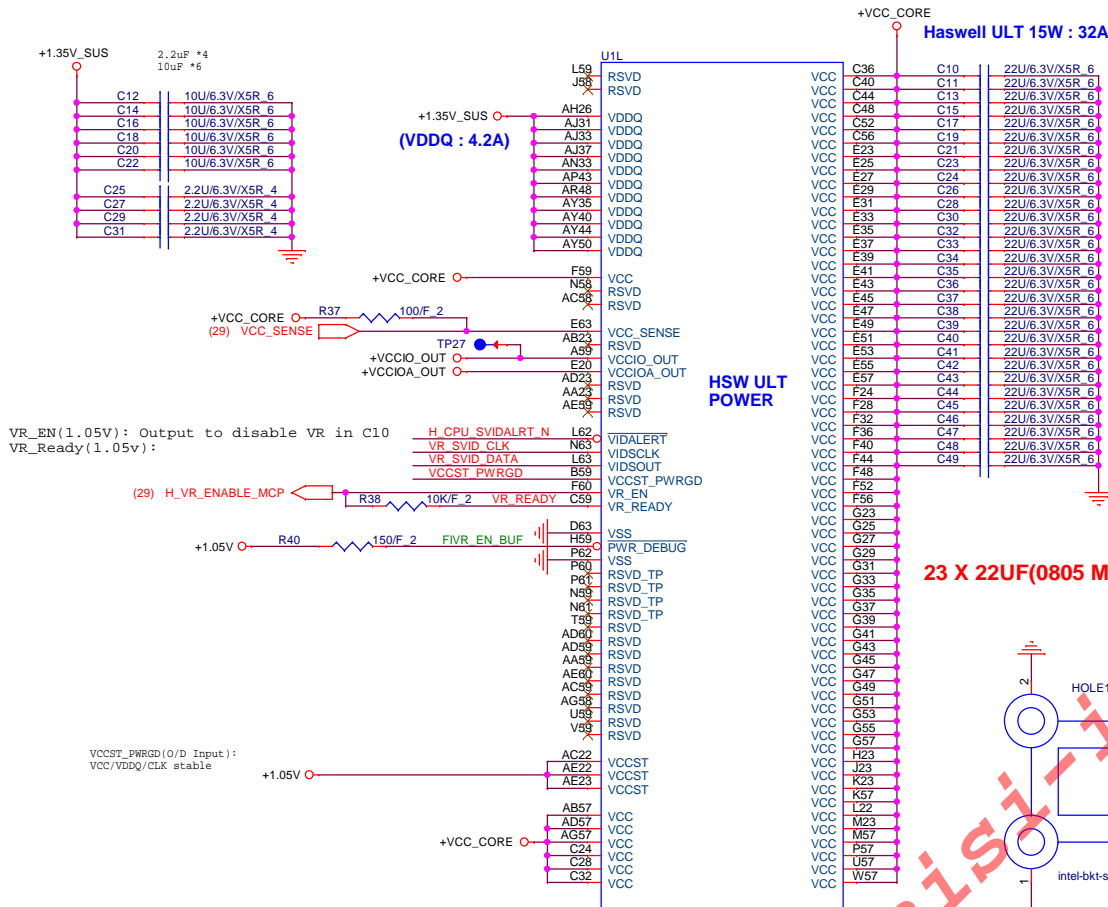
Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	



Broadwell U MCP(POWER)

07



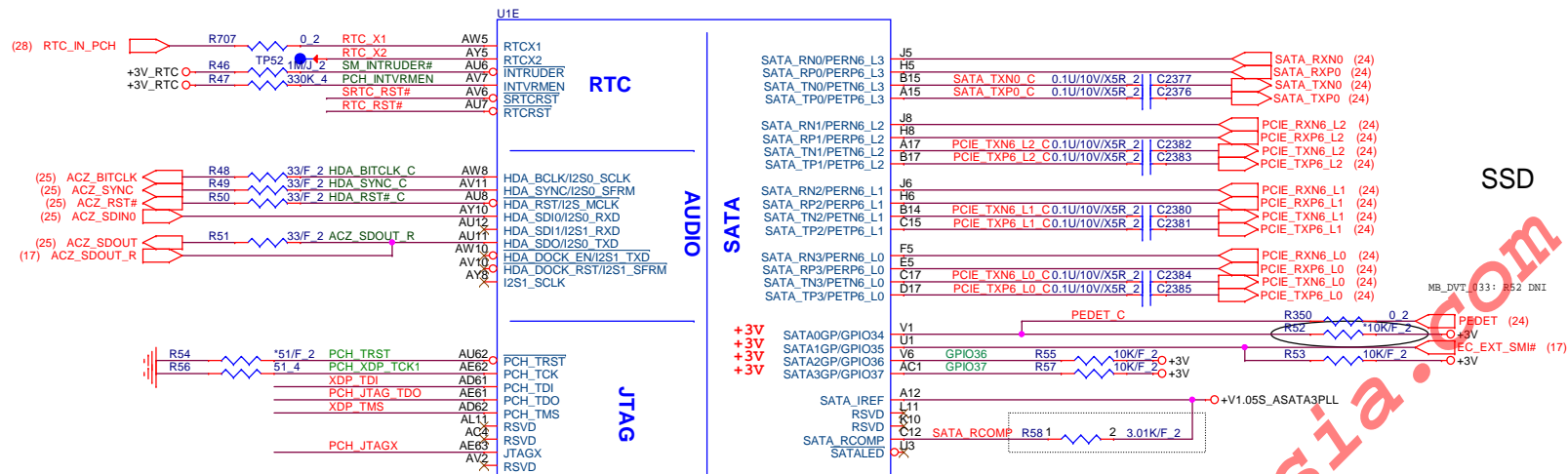
This part should not contain any substances which are specified in EM-S303.



Quanta Computer Inc.
PROJECT : MS8

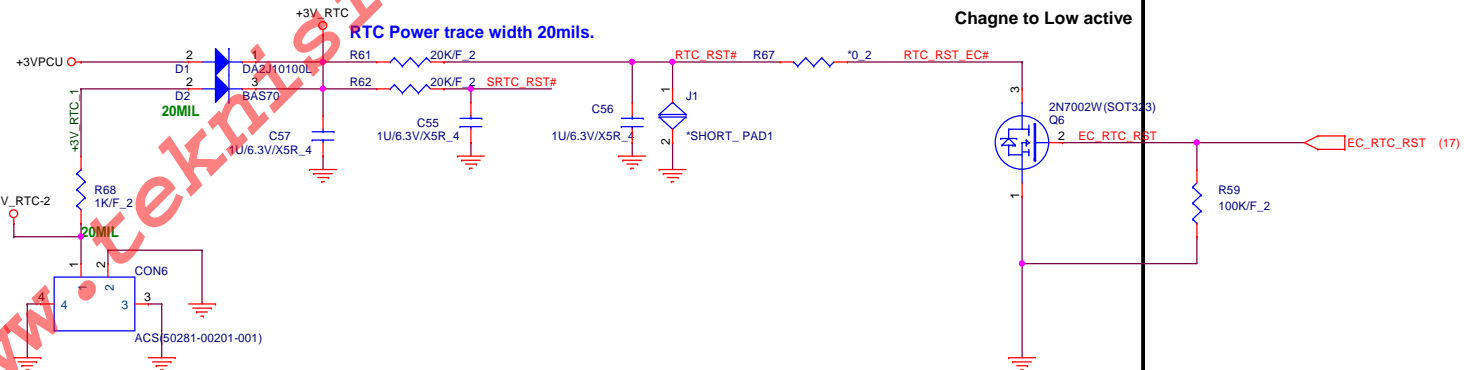
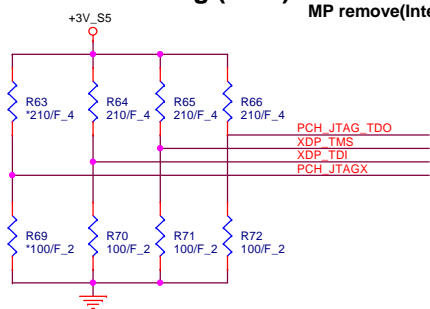
Size	Document Number	Rev
		1A
Date:	Wednesday, December 24, 2014	Sheet 7 of 36

BDW MCP(Power)



PCH JTAG Debug (CLG)

MP remove(Intel)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V _O R73 1K/F_2 SPKR (11)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTRVMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

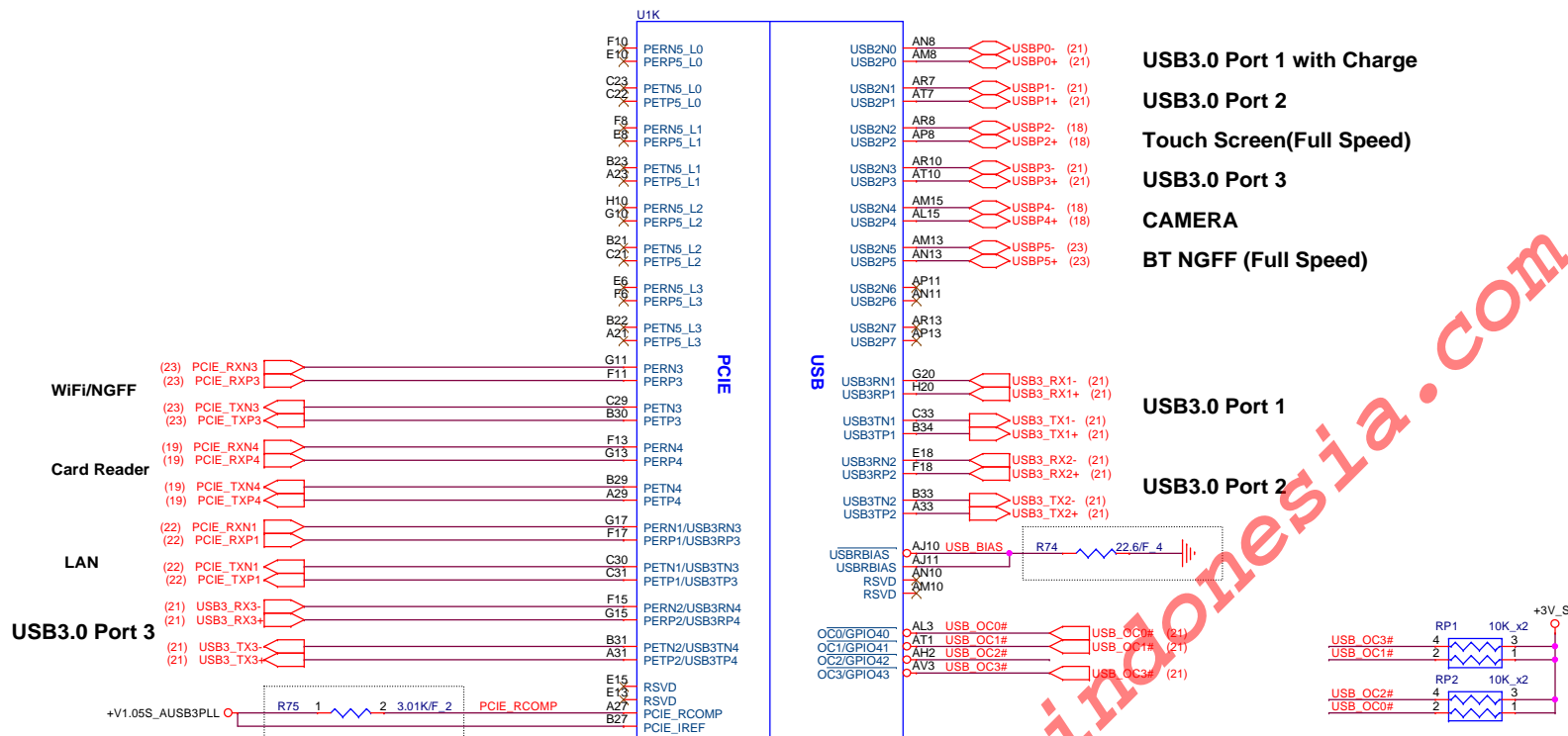
This part should not contain any substances which are specified in EM-S303.



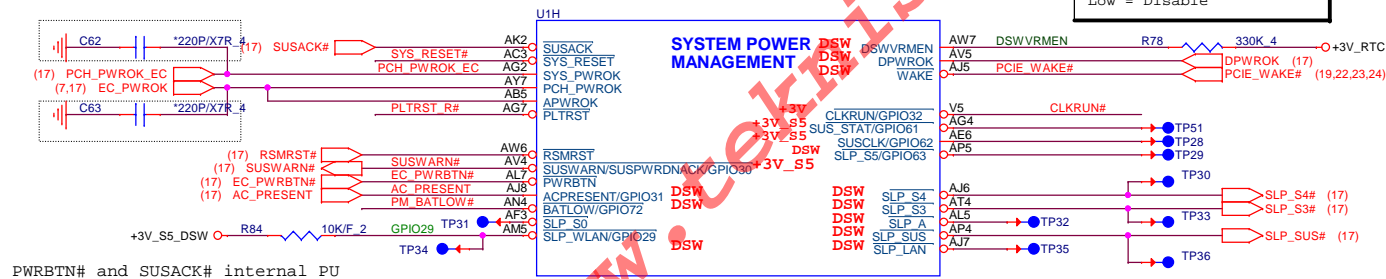
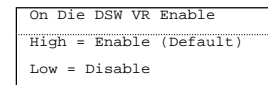
Quanta Computer Inc.
PROJECT : MS8

Size Document Number
BDW PCH(RTC/HDA/SATA)
Date: Wednesday, December 24, 2014 Sheet 8 of 36 Rev 2A

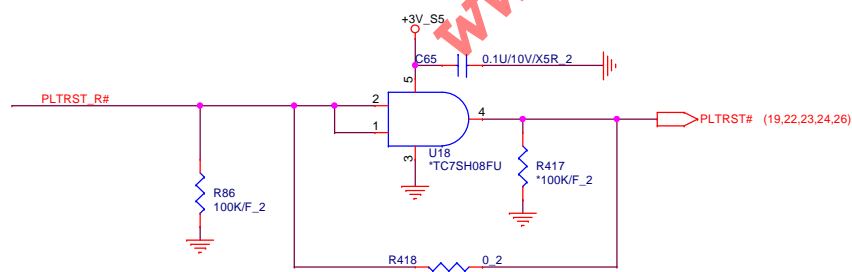
Broadwell U(PCIE,USB)



Broadwell U(SYSTEM POWER MANAGEMENT)

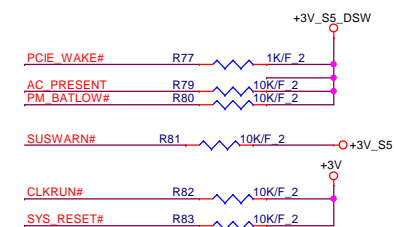


PWRBTN# and SUSACK# internal PU

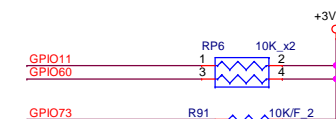
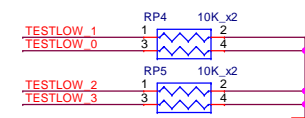
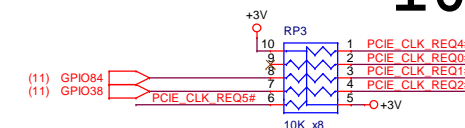
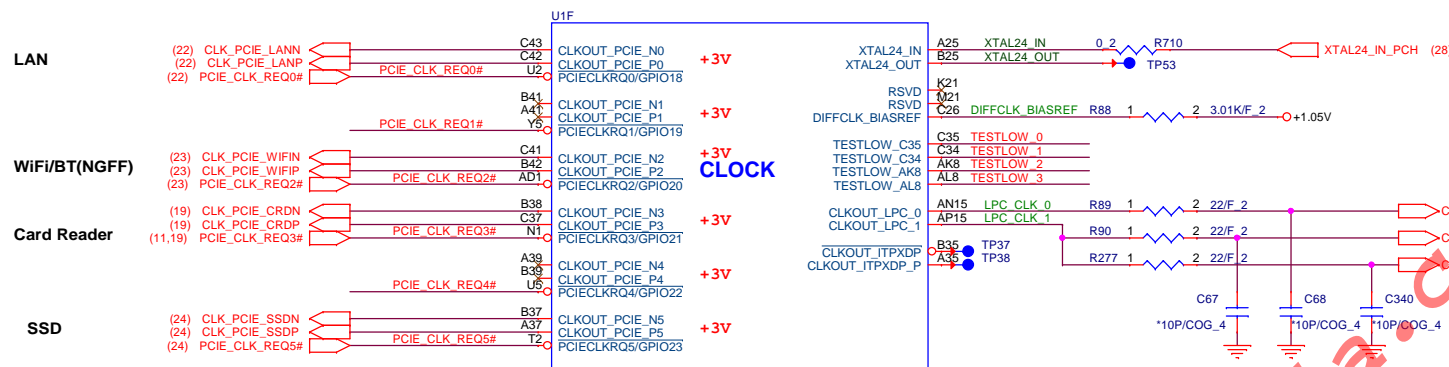


This part should not contain any substances which are specified in EM-S303.

PCH Pull-high/low(CLG)

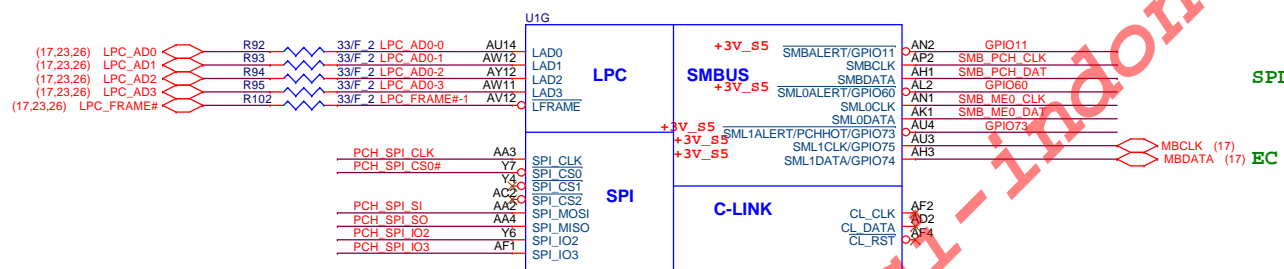


Broadwell U(CLK)

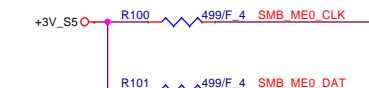
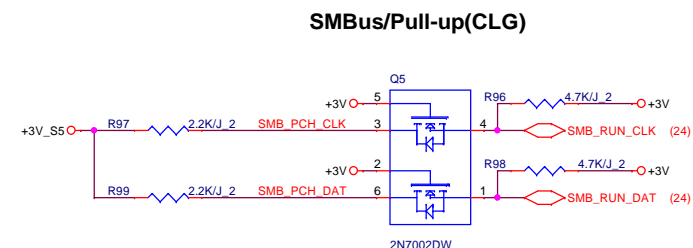


Do not short
the testlow
pins
together.

Broadwell U(LPC/SPI/SMB/CLINK)

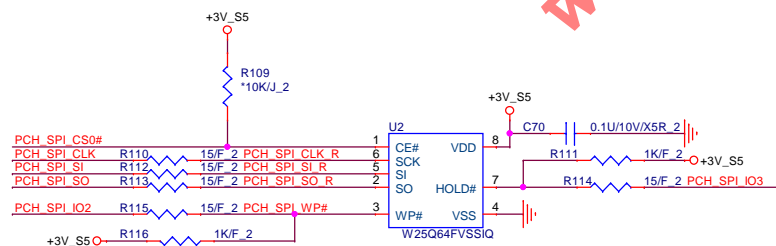


SPI



For NPCE985L Using

SPI FLASH

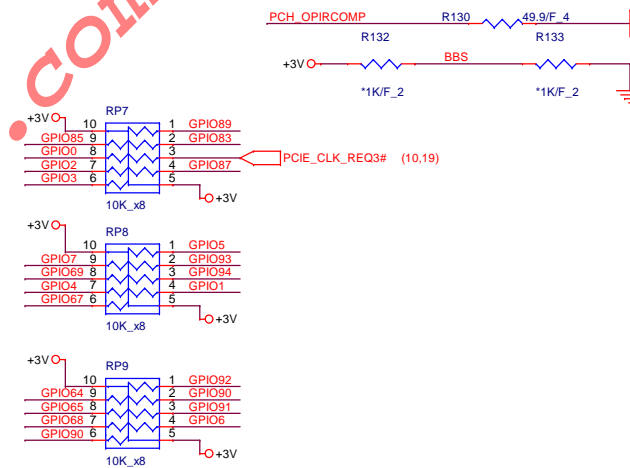
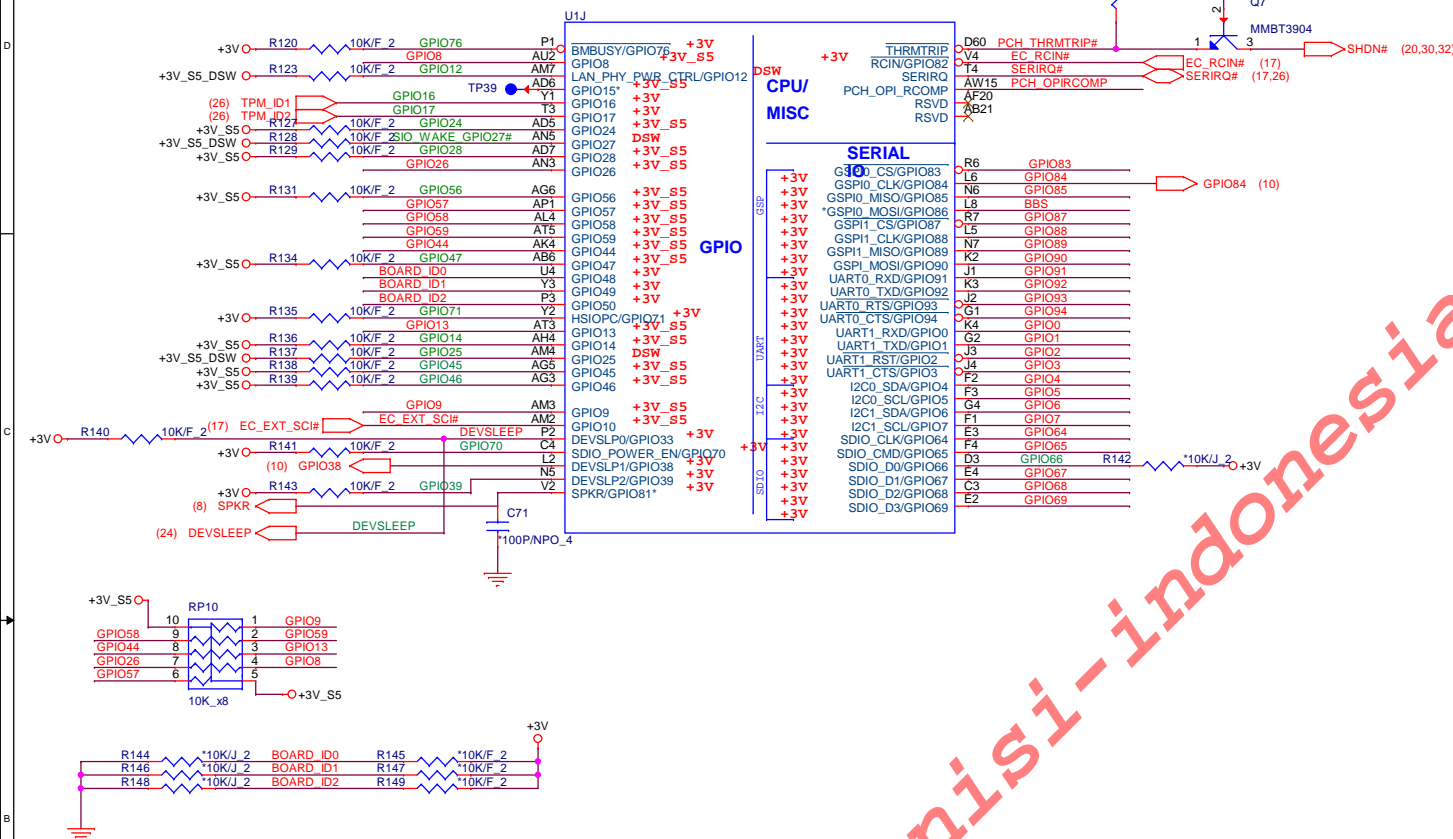


GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSW

Broadwell U(GPIO,LPIO,MISC)

GPIO Pull-up/Pull-down(CLG)



Vendor	Vendor Part Number	VIO P/N	BOARD_ID0	BOARD_ID1	BOARD_ID2
Micron(8G)	MT41K512M16HA-125:A	AKD5QGSTL03	0	0	0
Samsung(8G)	K4B8G1646Q-MYK0	AKD5QGST505	0	0	1
Hynix(8G)			0	1	0
Micron(4G)	MT41K256M16HA-125:A	AKD5JGSTL20	0	1	1
Samsung(4G)	K4B4G1646Q-HYK0	AKD5PGST518	1	0	0
Hynix(4G)	H5TC4G63AFR-PBA	AKD5JGETW20	1	0	1
			1	1	0
Elpida(8G)	EDJ8416E6MB-GN-F	AKD5FGST411	1	1	1

This part should not contain any substances which are specified in EM-S303.

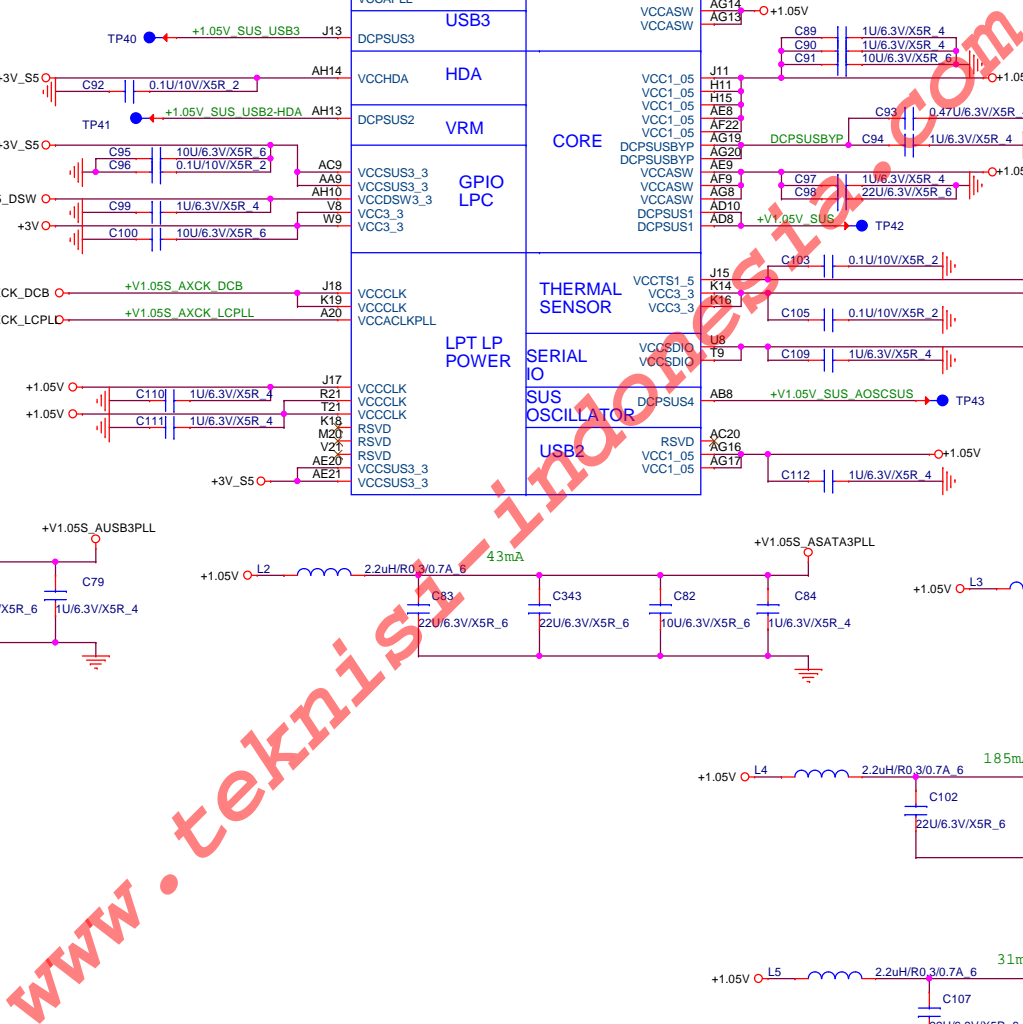
GPIO66 Top-Block Swap	
PU	Enable
PD	Disable(Default) internal weak pull-dpwn


GPIO86	
PU	LPC
PD	SPI (Default IPD)

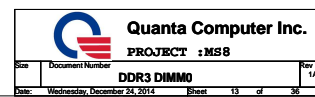
No Reboot Strap(GPIO81)	
NC	Default
PU	EN

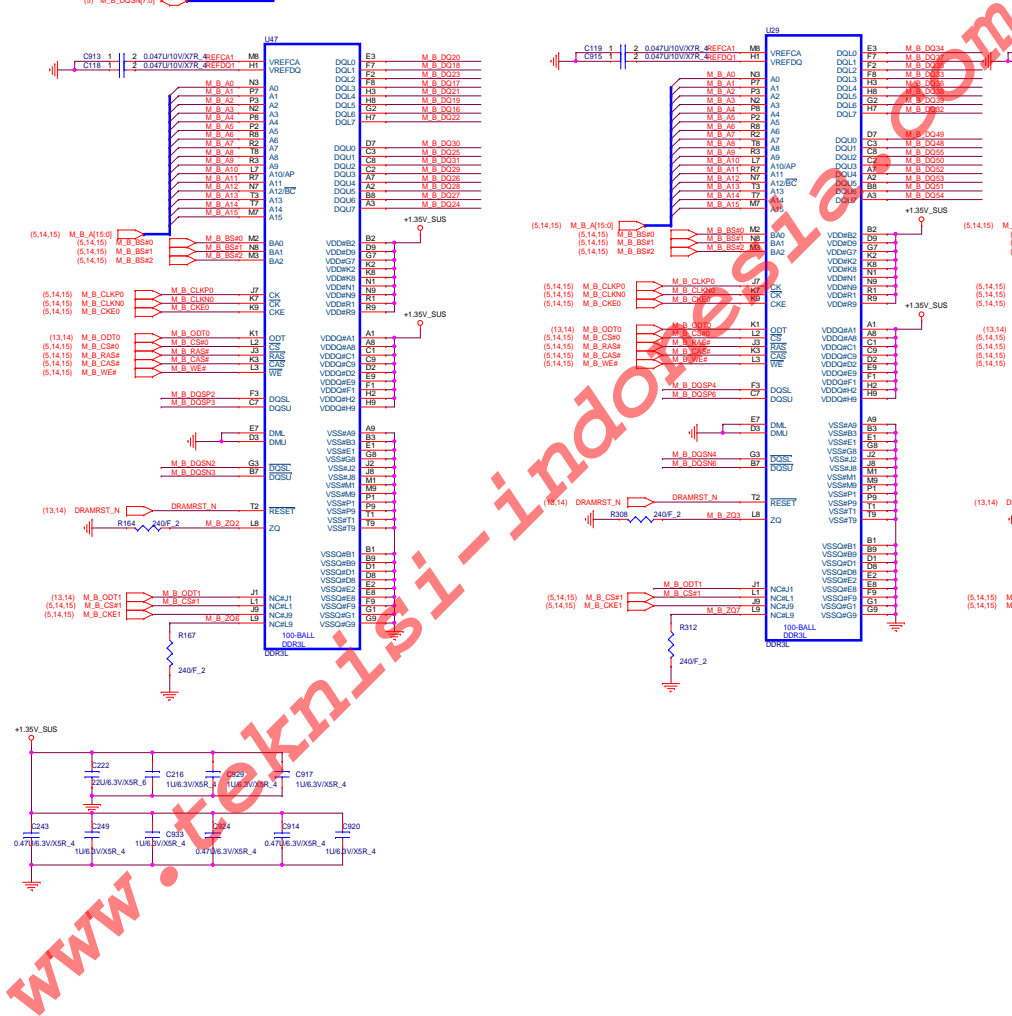
TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

		PROJECT : MS8	
		BDW PCH(GPIO/MISC)	
Size	Document Number	Date	Wednesday, December 24, 2014
Sheet	11	of	36
Rev	1A		

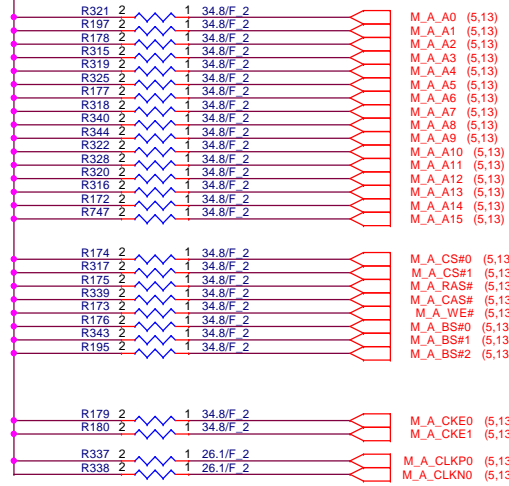


		Quanta Computer Inc. PROJECT : MS8	
Size	Document Number	Rev 1A	
BDW PCH(Power)		Date: Wednesday, December 24, 2014	
		Sheet 12 of 36	

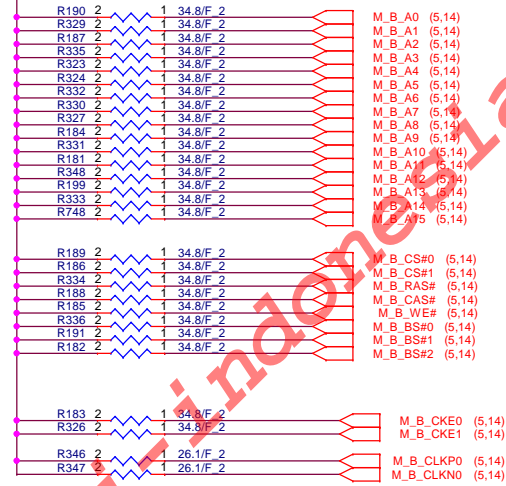




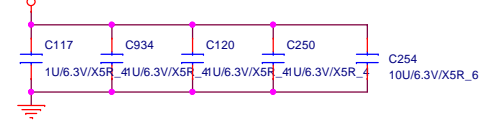
+0.675V_DDR_VTT



+0.675V_DDR_VTT



+0.675V_DDR_VTT



This part should not contain any substances which are specified in EM-S303.

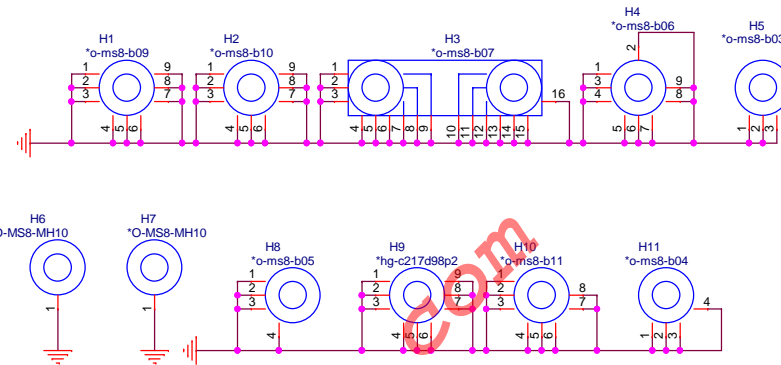
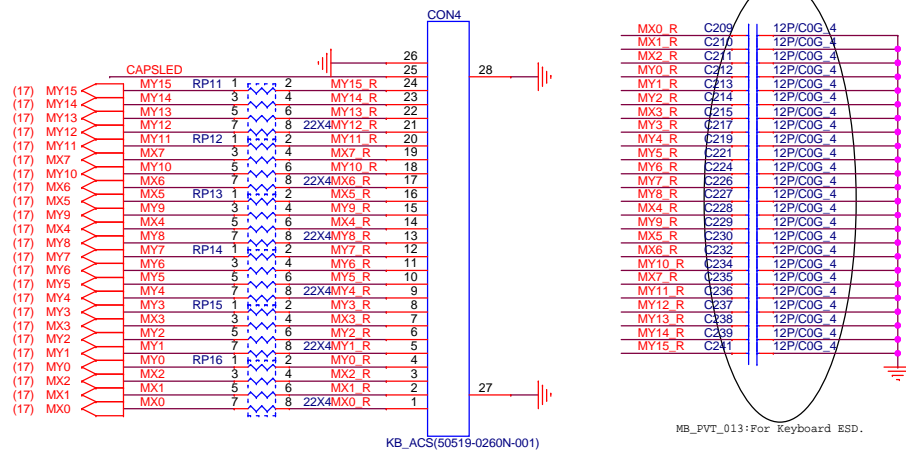


Quanta Computer Inc.

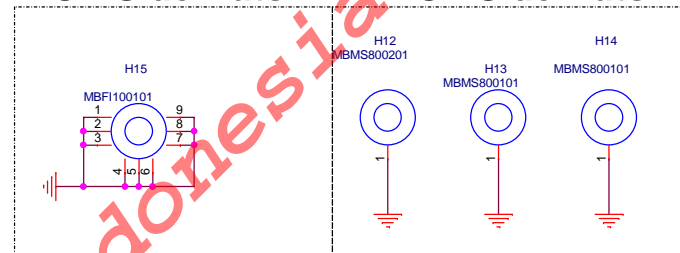
PROJECT : MS8

Size	Document Number	Rev
	DDR3L TERMINATION	1A
Date:	Wednesday, December 24, 2014	Sheet 15 of 36

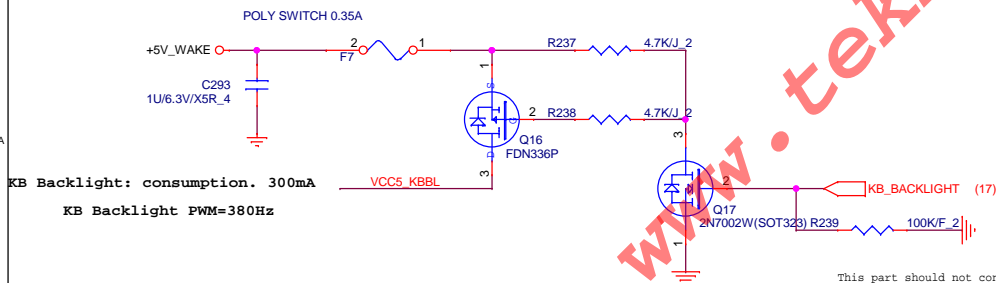
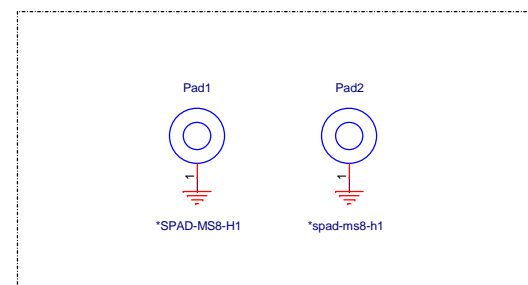
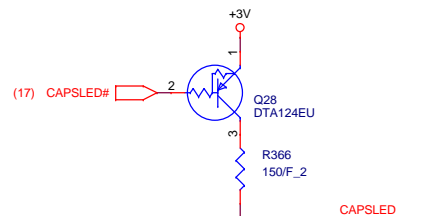
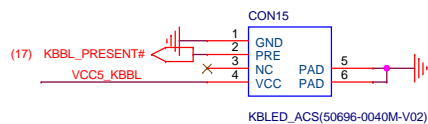
KEY BOARD Connector



TOP Side Nuts BOT Side Nuts

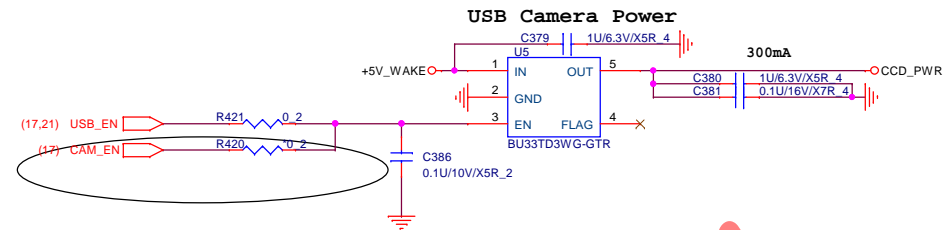


KB BACKLIGHT

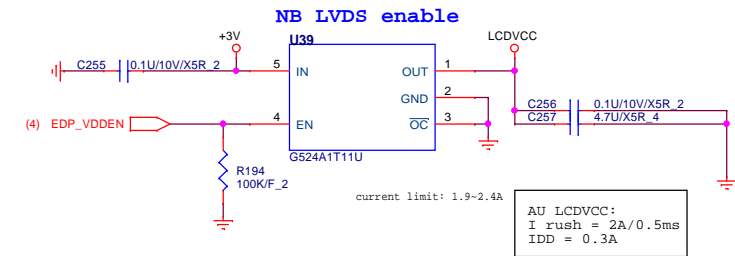
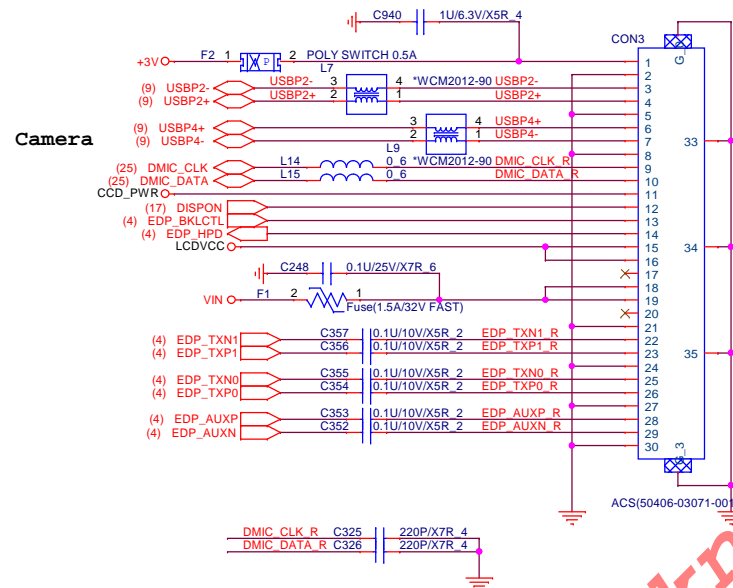


This part should not contain any substances which are specified in EM-S303.

		Quanta Computer Inc. PROJECT : MS8	
Size	Document Number	HOLE/EMI/KB	
Date:	Wednesday, December 24, 2014	Sheet	16 of 36



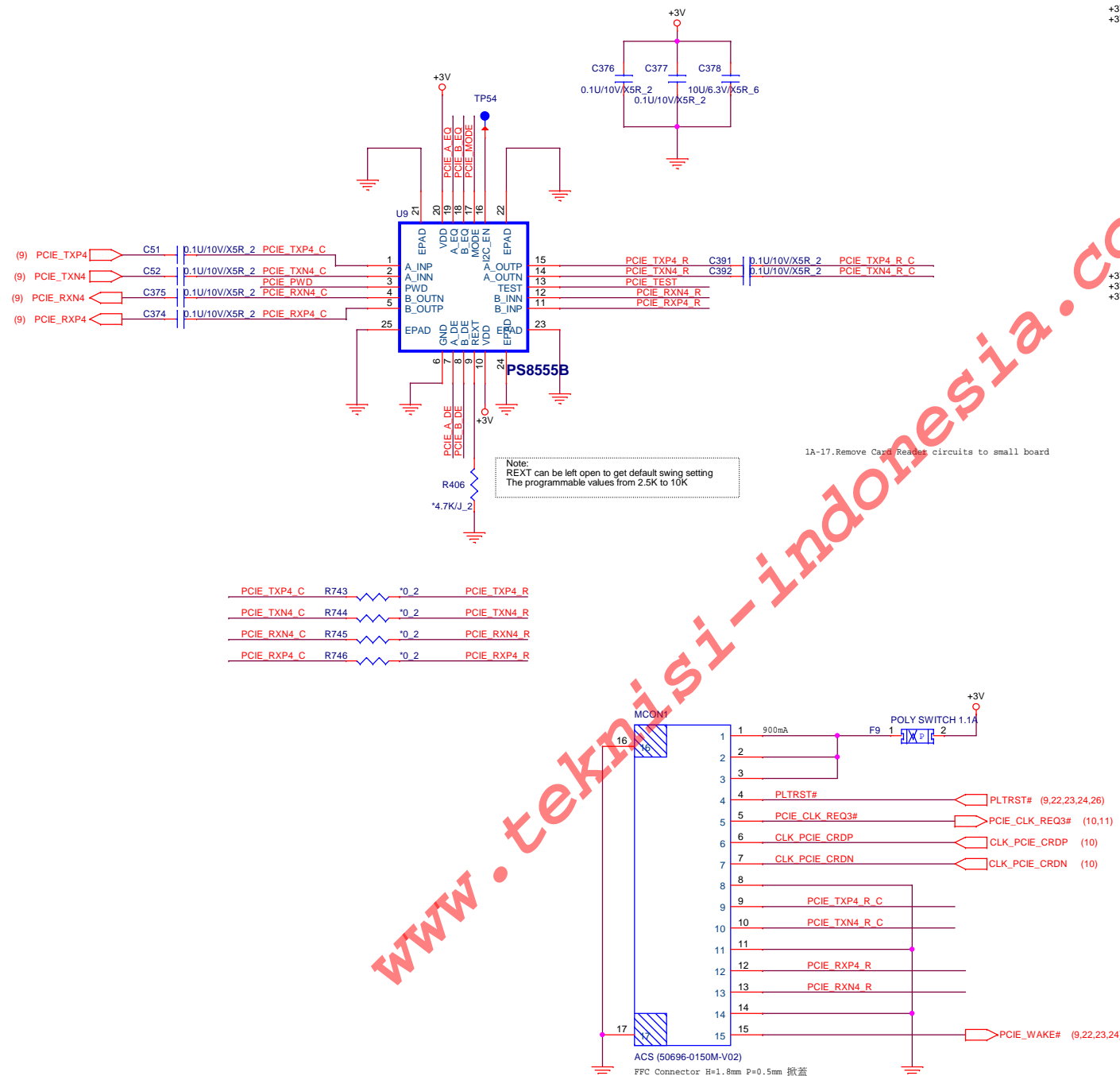
eDP+Touch Scean+Camera



GND Pin Distribute

	Pin number
TouchScreen	Pin2&Pin5
Camera	Pin8
Backlight of Panel	Pin21&Pin24
Logic circuits of Panel	Pin27&Pin30

This part should not contain any substances which are specified in EM-S303



+3V_{IO} R407 *4.7K/J 2 PCIE_A_DE
+3V_{IO} R408 *4.7K/J 2 PCIE_B_DE

Programmable output de-emphasis level setting for channel A/B at pin control mode. 3.3V tolerant. Internally pulled down at ~150K.
[A/B_DE] ==
L: 1.5dB de-emphasis(default)
H: 3.5dB de-emphasis

PCIE_A_EQ R415 *4.7K/J 2
PCIE_B_EQ R416 *4.7K/J 2

Equalizer control and program for channel A/B at pin control mode. 3.3V tolerant.
Internally pulled up at ~150K.
[A/B_EQ] ==
L: program EQ for channel loss up to 4.5dB
H: program EQ for channel loss up to 13dB(default)

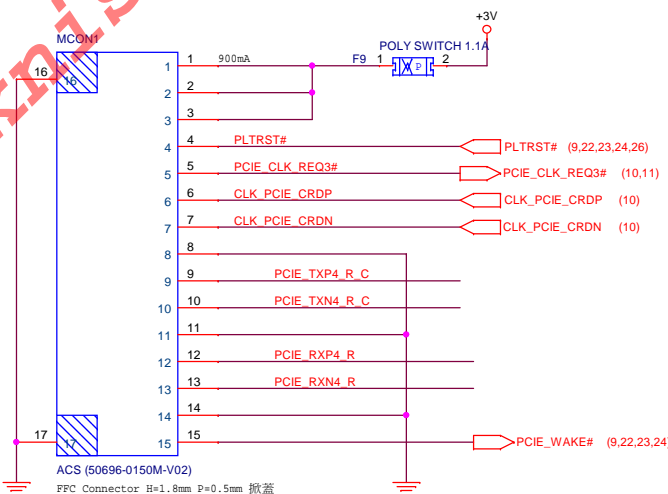
+3V_{IO} R411 4.7K/J 2 PCIE_MODE
+3V_{IO} R412 *4.7K/J 2 PCIE_TEST
+3V_{IO} R413 *4.7K/J 2 PCIE_PWD

Mode selection. 3.3V tolerant. Internally pulled down at ~150K.
MODE ==
L: SATA operation mode (default)
H: PCIe operation mode

Compliance testing configuration. 3.3V tolerant. Internally pulled down at ~150K.
TEST ==
L: Normal operation (default)
H: Compliance Testing mode enable

Chip power down. 3.3V tolerant. Internally pulled down at ~150K.
PWD ==
L: Normal operation (default)
H: Chip power down.

1A-17.Remove Card Reader circuits to small board



This part should not contain any substances which are specified in EM-S303.

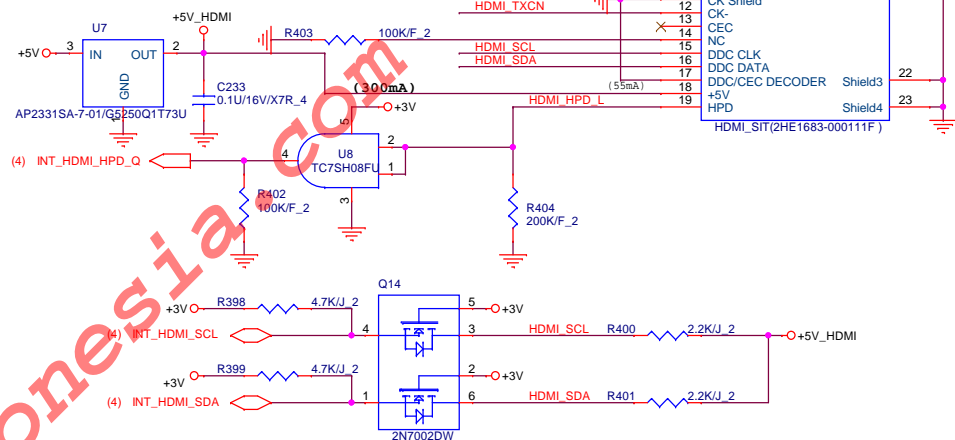
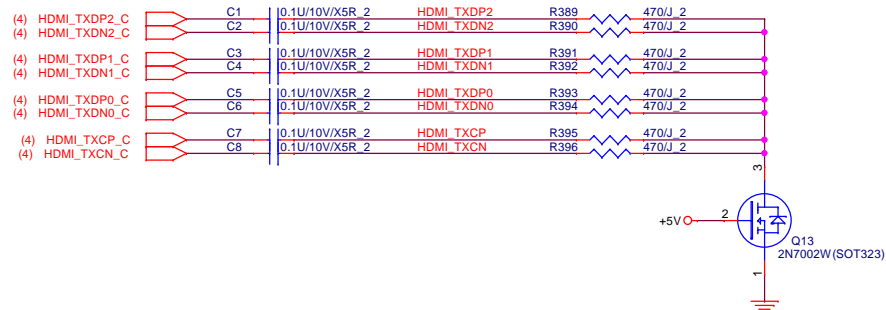
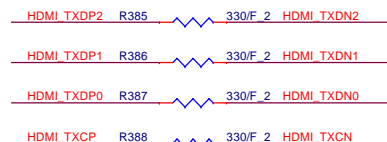


Quanta Computer Inc.

PROJECT : MS8

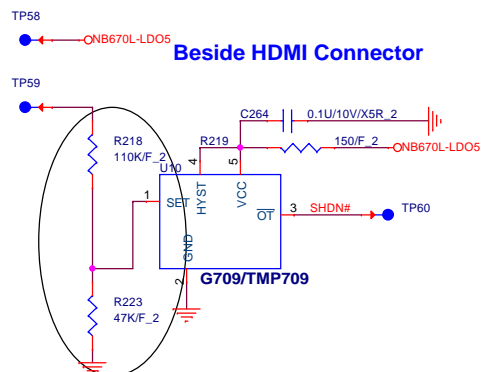
Cared Reader SamII Board

Size	Document Number	Rev
		1A
Date:	Wednesday, December 24, 2014	Sheet 19 of 36



H/W Thermal Protect

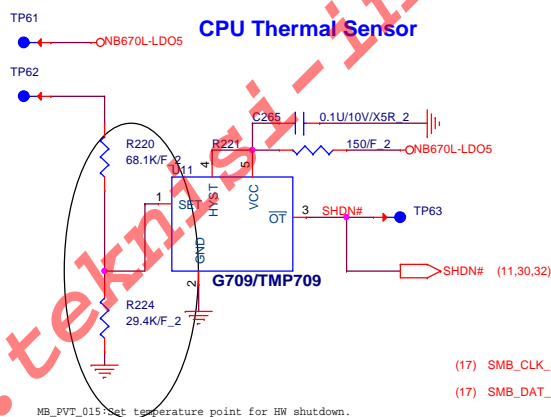
CPU Thermal Sensor



MB_PVT_015:Set temperature point for HW shutdown.

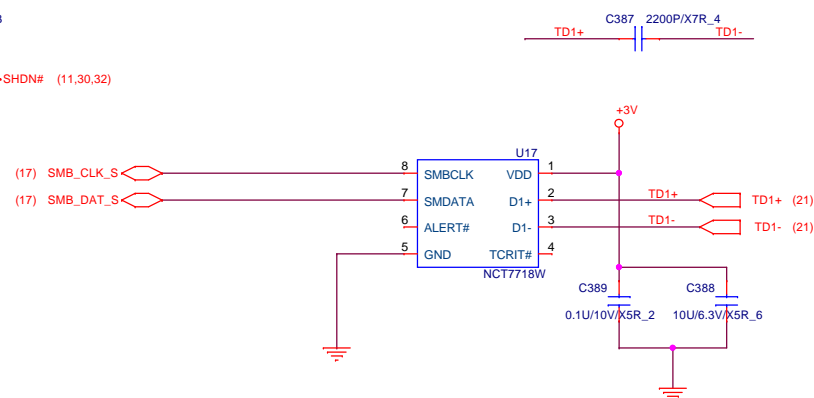
$$RSET(k\Omega) = 0.0012T2 - 0.9308T + 96.147$$

57	47K
80	29.4K
107	10.3K
110	8.2K



MB_PVT_015:Set temperature point for HW shutdown.

H/W Thermal sensor



UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp		R223=10K		105	105
Near AUDIO sensor temp		R224=10K		105	105

This part should not contain any substances which are specified in EM-S303.



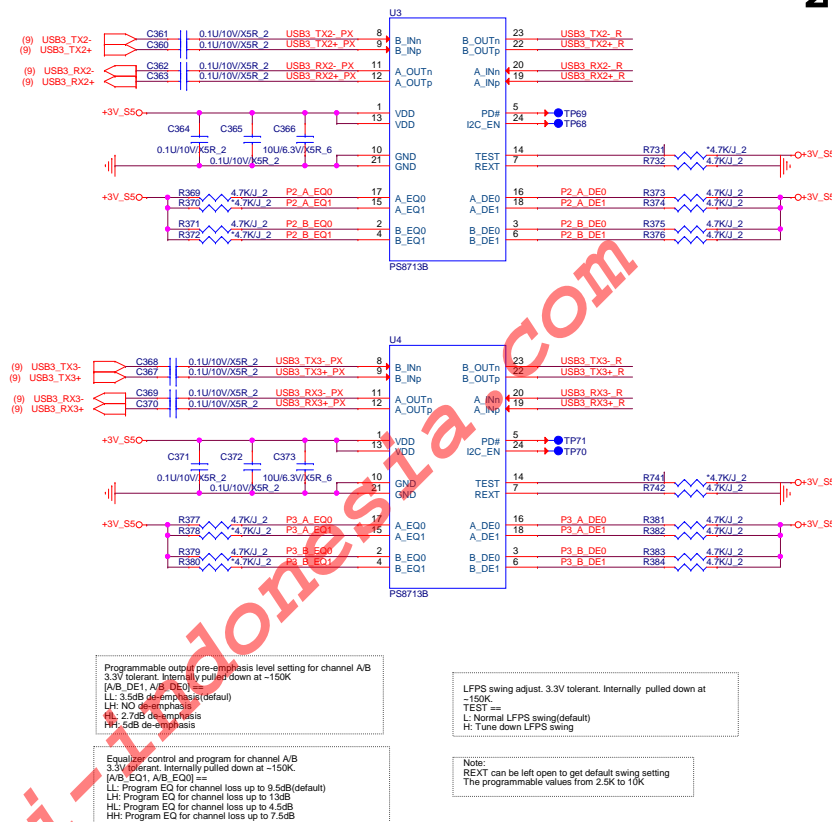
Quanta Computer Inc.

PROJECT : MS8

HDMI/Thermal IC

Size	Document Number	Rev
		2A

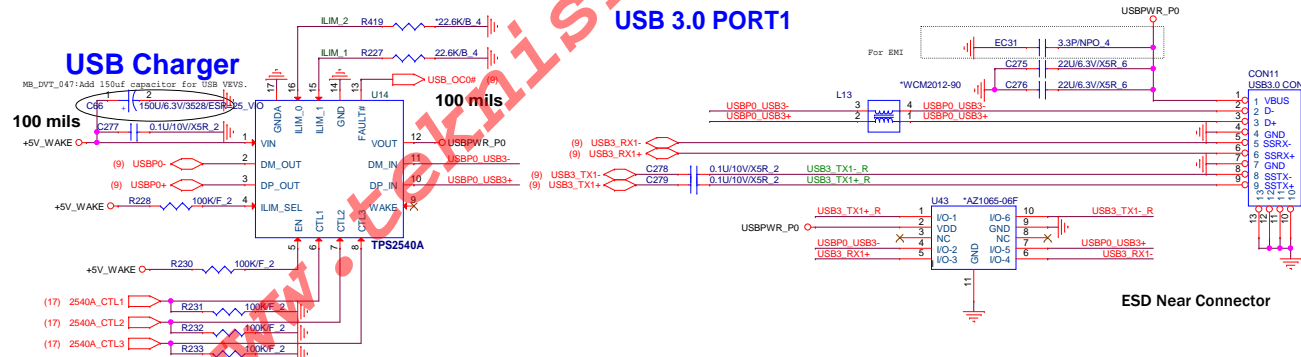
Date: Wednesday, December 24, 2014 Sheet 20 of 36




Mode CDP OFF DCP

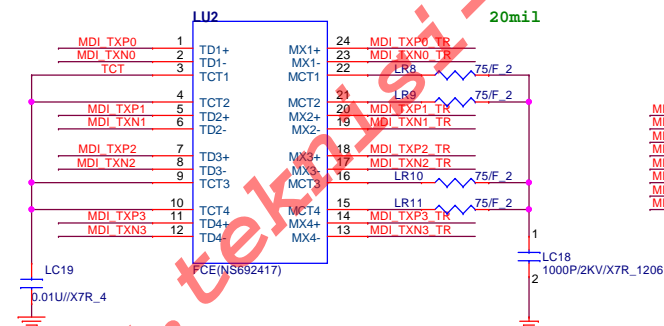
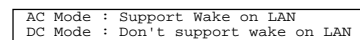
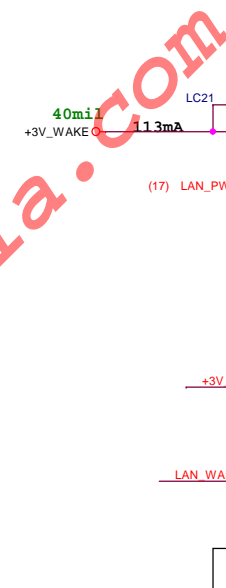
VBUS

VBUS stop time 1Sec



System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

 Quanta Computer Inc. PROJECT : MS8		Rev 2A
Size	Document Number	
USB/USB Charger		
Date:	Wednesday, December 24, 2014	Sheet 21 of 36



Quanta Computer Inc.
PROJECT : MS8

NGFF Wifi/BT

+3.3V_NGFF_WLAN
Max Current : 1000mA

23

Blue Tooth

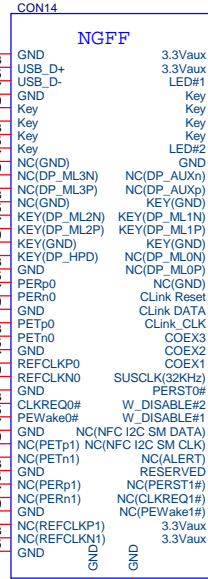
(9) USBP5+
(9) USBP5-

WIFI

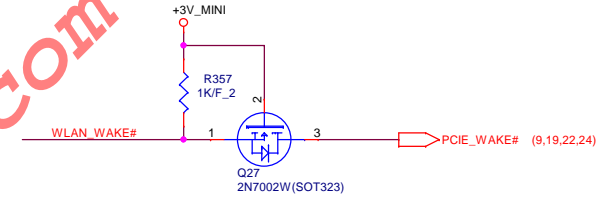
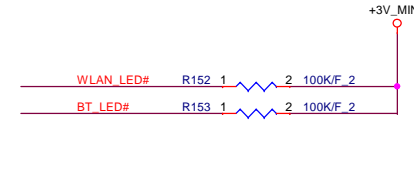
(9) PCIE_TXP3
(9) PCIE_TXN3
(9) PCIE_RXP3
(9) PCIE_RXN3

(10) CLK_PCIE_WIFIP
(10) CLK_PCIE_WIFIN
(10) PCIE_CLK_REQ2#

(10) CLK_PCL_LPC
(10,17,26) LPC_FRAME#



WLAN_NGFF_CONN_LTS(APC10147-P007A)



WLAN+Bluetooth
20 : Internal Pull high 25K ~ 58K

www.teknisi-indonesia.com

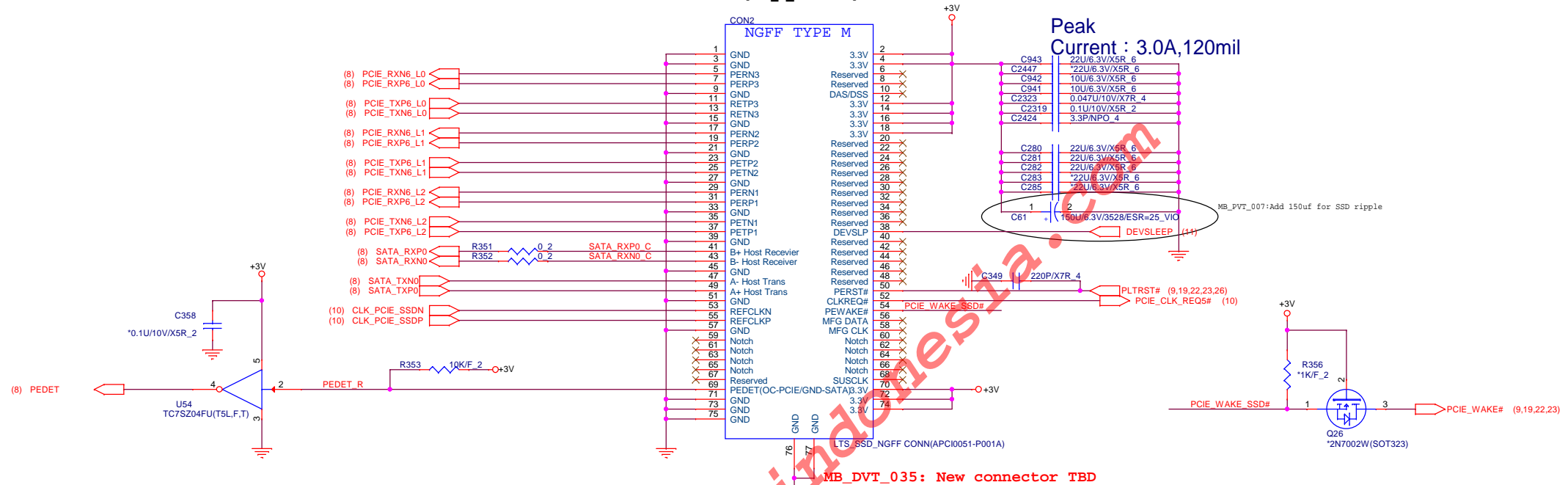


Quanta Computer Inc.
PROJECT : MS8

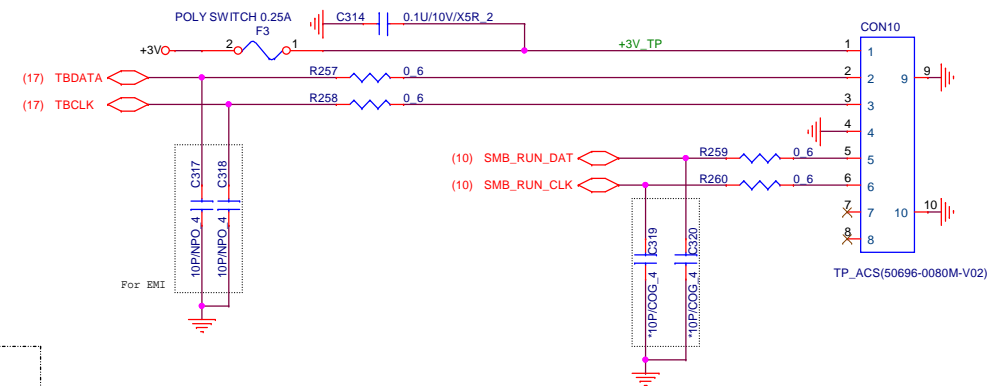
Size	Document Number	Rev
	WLAN	1A
Date:	Wednesday, December 24, 2014	Sheet 23 of 36

This part should not contain any substances which are specified in EM-S303.

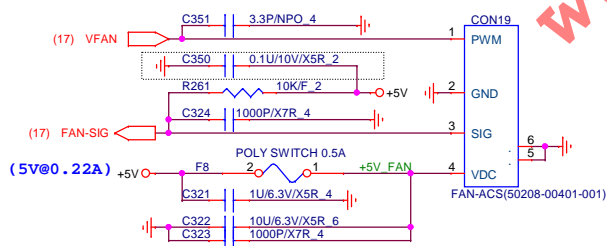
SSD CONNECTOR (Type M)



T/P Board to T/P



MAIN FAN

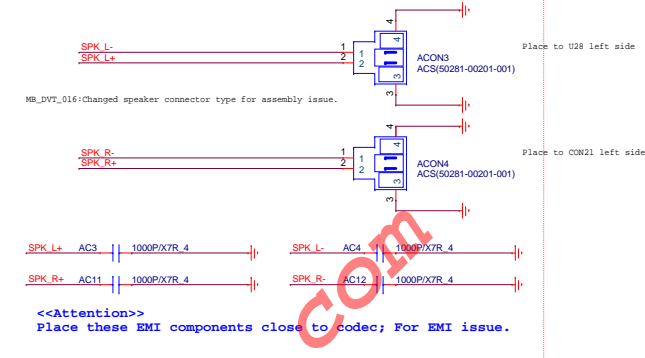


Pin No.	Signal	Note	Lead Color
1	PWM	---	WHITE
2	GND	---	BLACK
3	SIG	FG OUT (2Pulses/rev) (Open Collector)	GRAY
4	VDC	+5V	RED

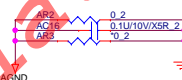
This part should not contain any substances which are specified in EM-S303.



Quanta Computer Inc.
PROJECT : MS8

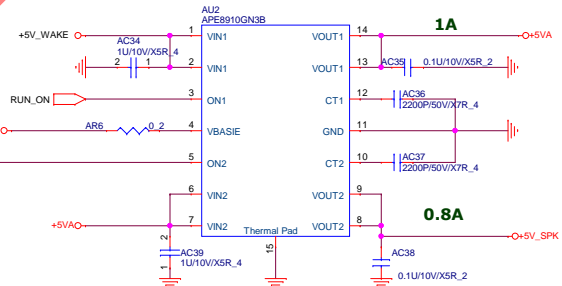


For EMI



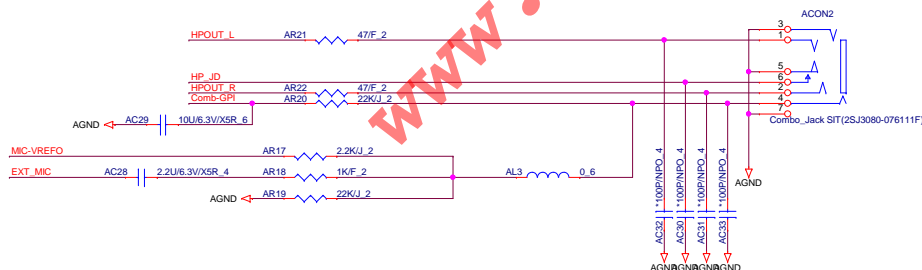
Analog

Digital



	DC_DET
Assert	Floting
De-assert	Pull down to GND

Combo Jack

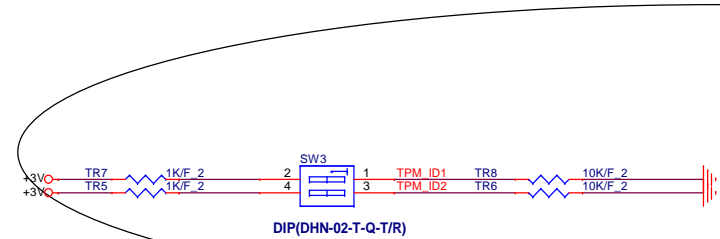
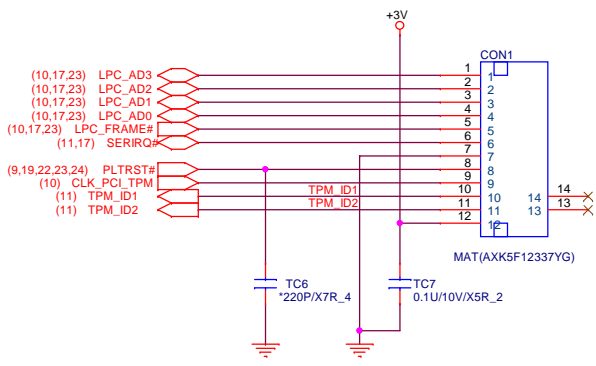


TPM BTB

TPM

MB_PVT_005:Remove TPM circuits on motherboard.

MB_PVT_021:Define TPM configuration



MB_PVT_006:Add TPM Switch for TPM version.

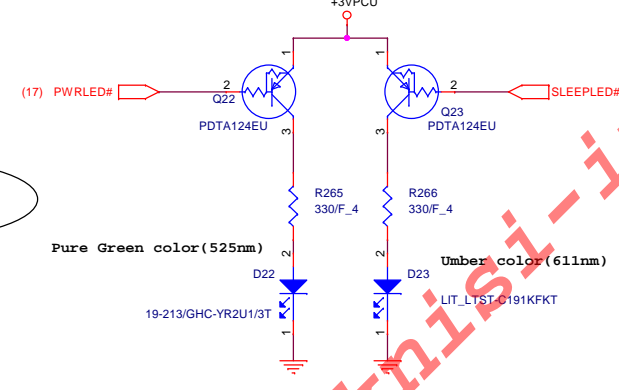
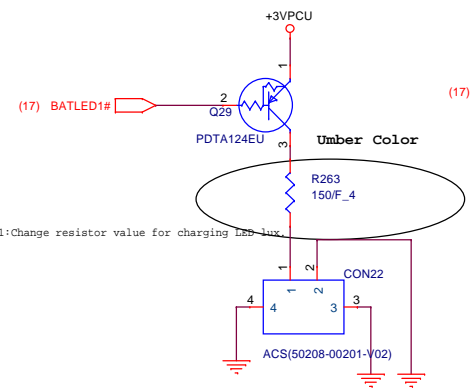
TPM_ID1	FW_VER
0	V1.2
1	V2.0

TPM_ID2	FW_VER
0	W/O TPM
1	W TPM

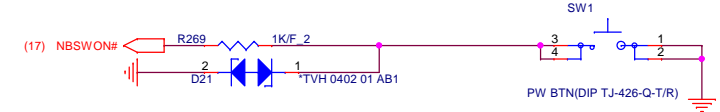
BATTERY LED

TPM BTB

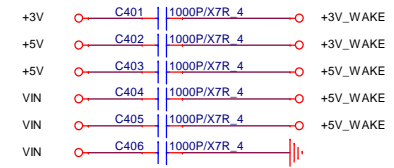
Power/Sleep LED



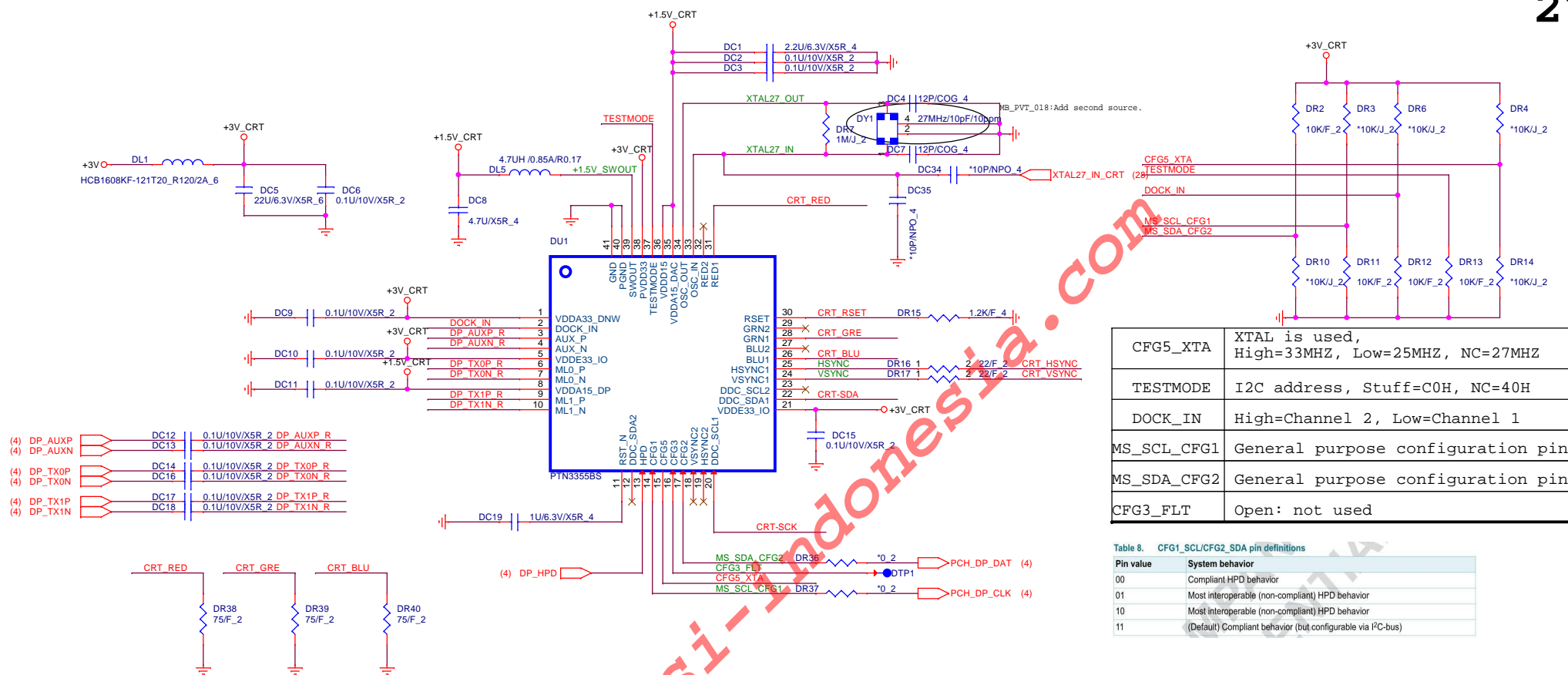
Power SW



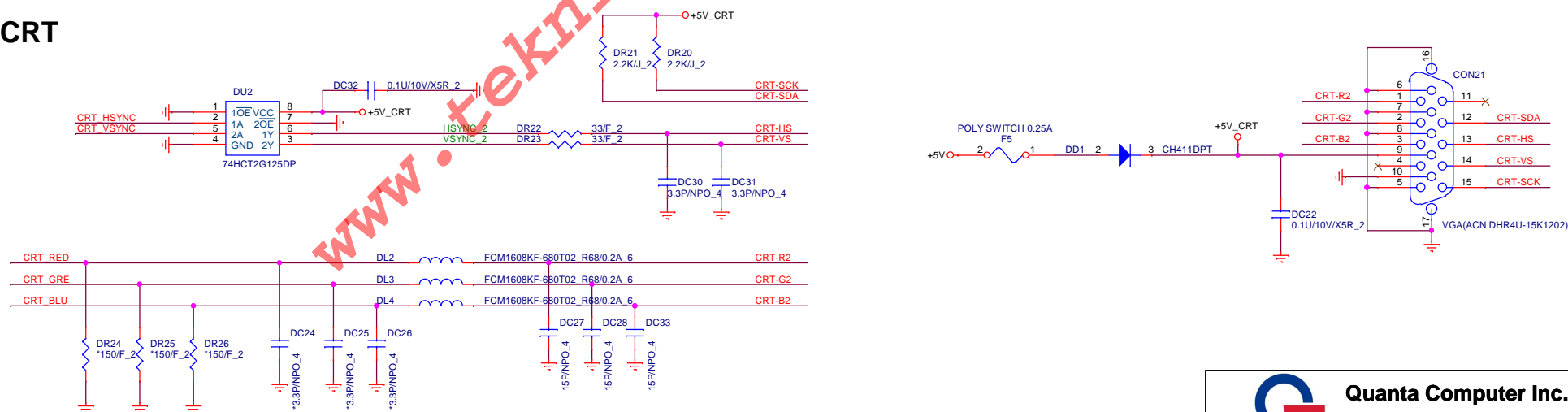
Cross Power Plane Capacitors



This part should not contain any substances which are specified in EM-S303.



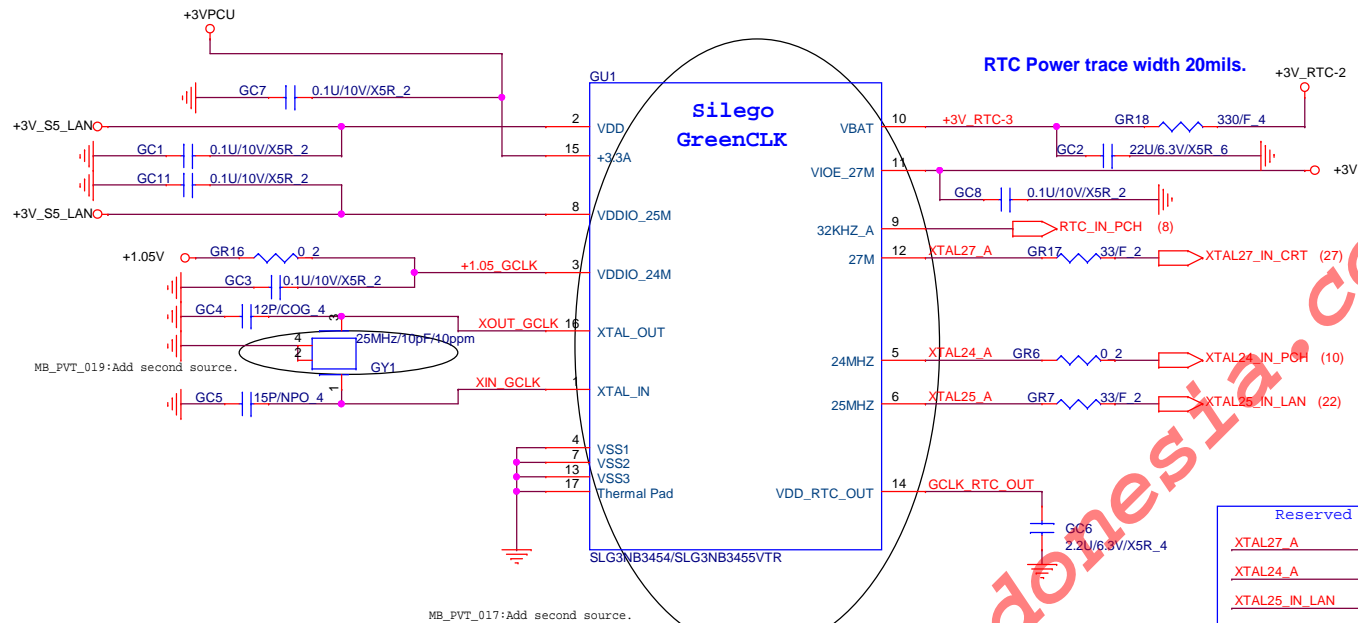
CRT



This part should not contain any substances which are specified in EM-S303.



Quanta Computer Inc.
PROJECT : MS8



MB_PVT_017: Add second source.

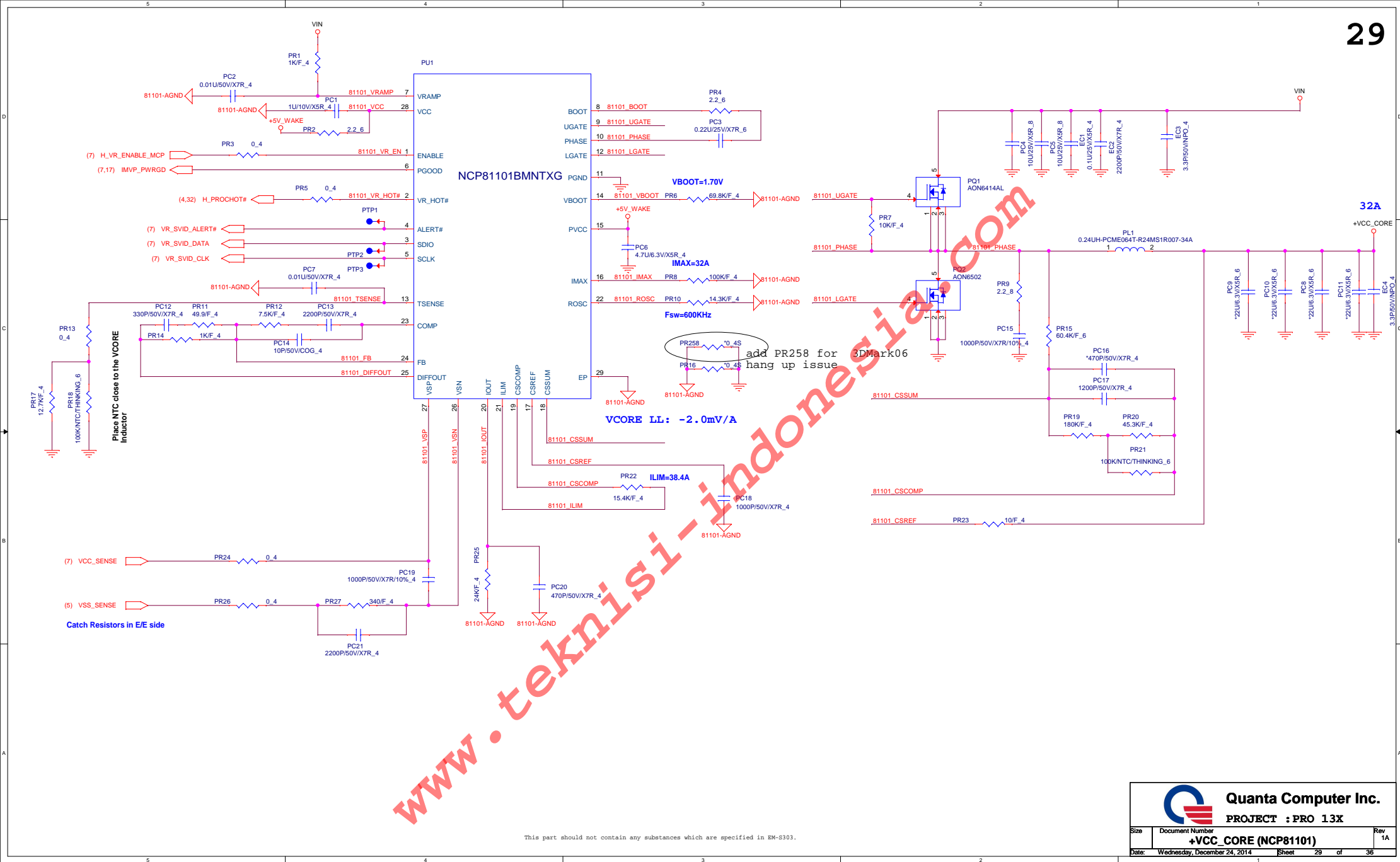
This part should not contain any substances which are specified in EM-S303.

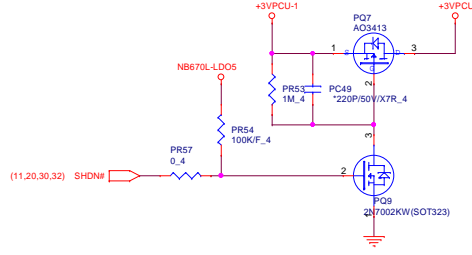
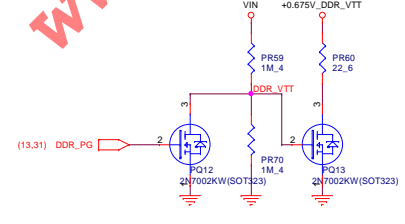
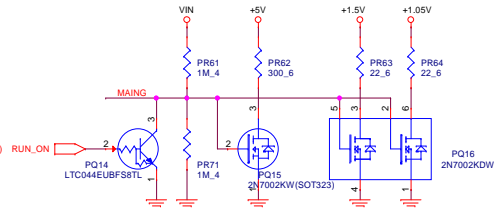
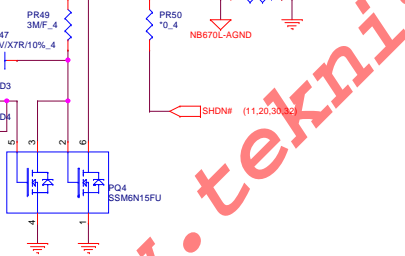
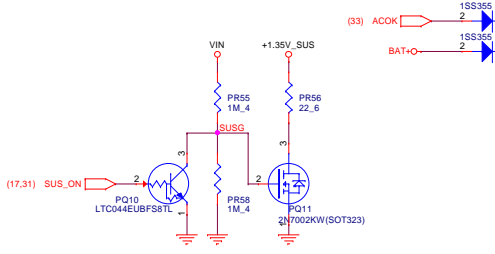
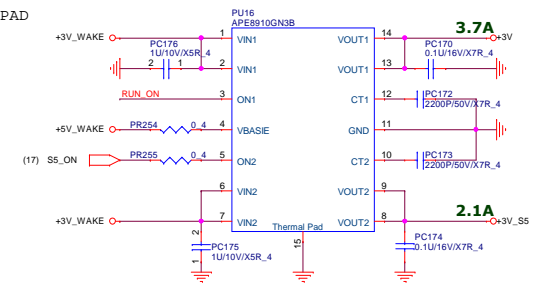
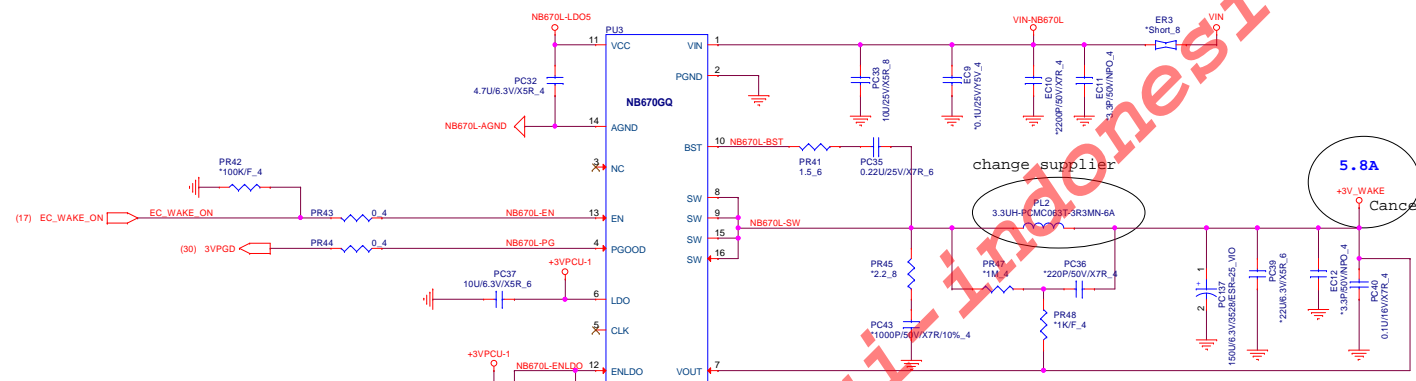
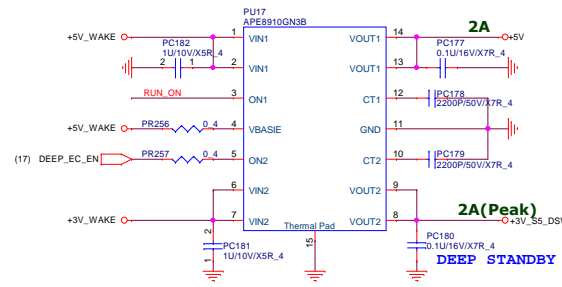
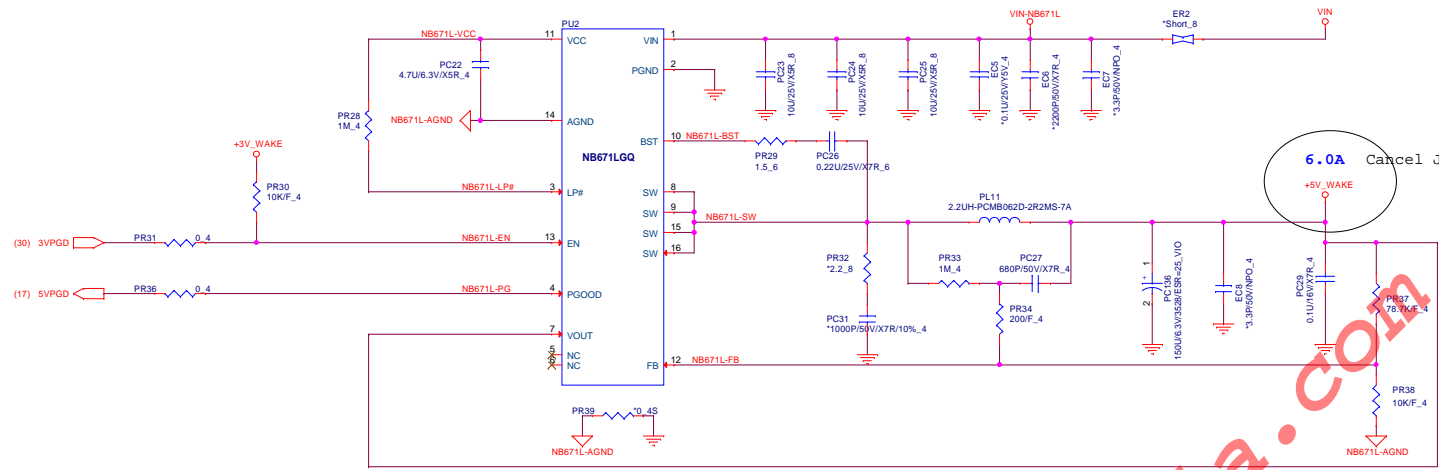


Quanta Computer Inc.

PROJECT :

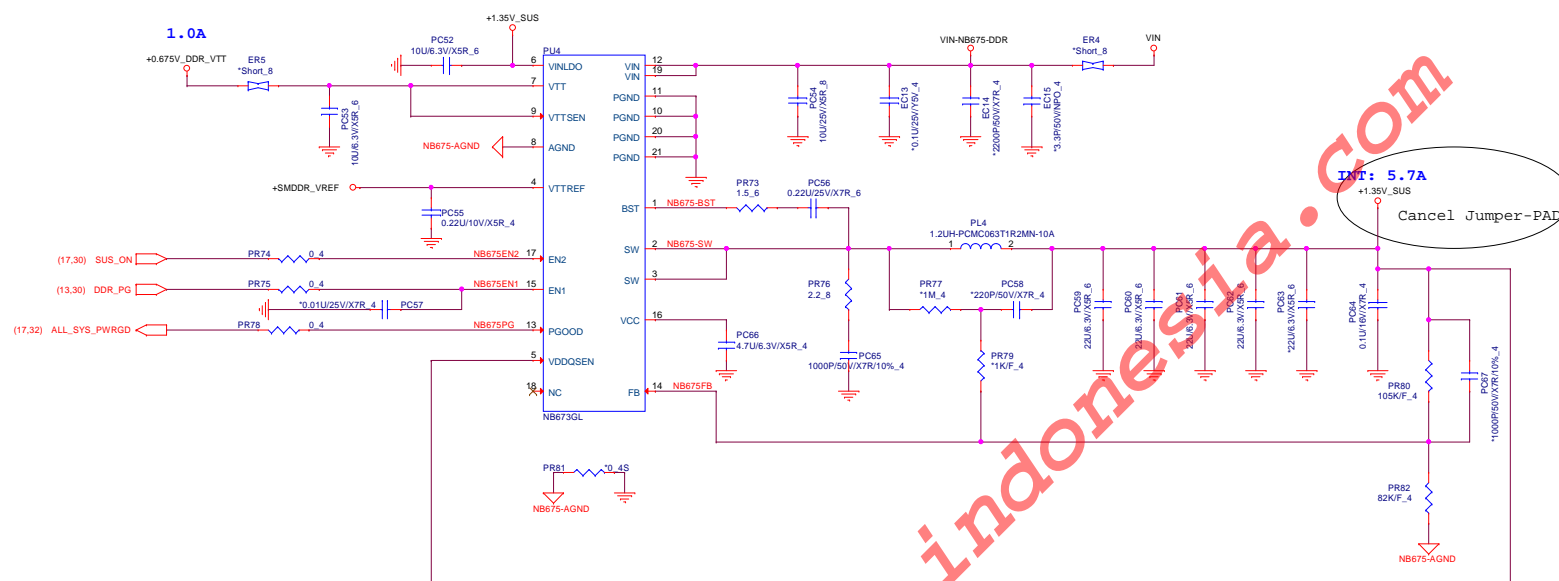
Size	Document Number	Rev
	GreenCLK(SLG3NB3454)	2A
Date:	Wednesday, December 24, 2014	Sheet 28 of 36



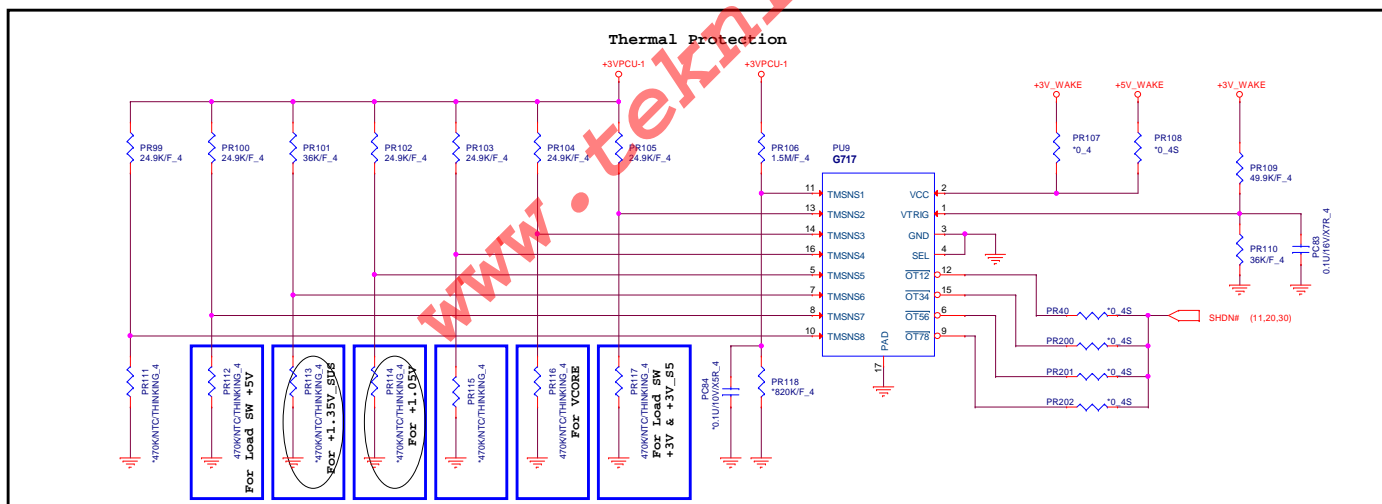
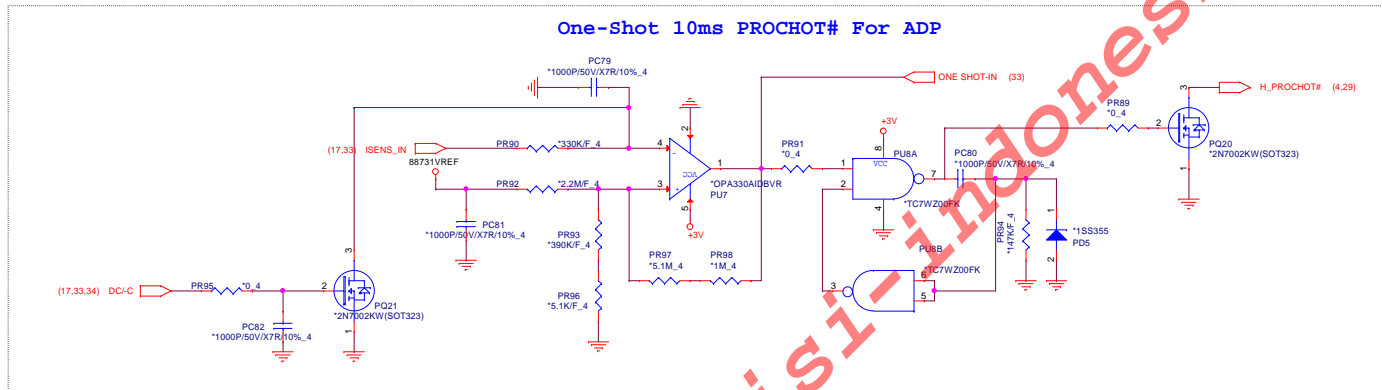
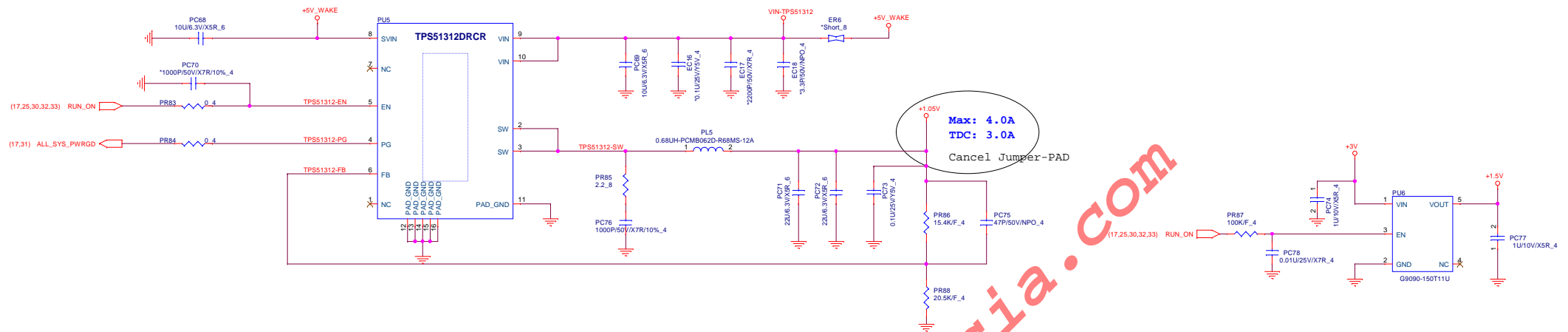


This part should not contain any substances which are specified in EN-8303.

1.35VSUS & VTT_MEM

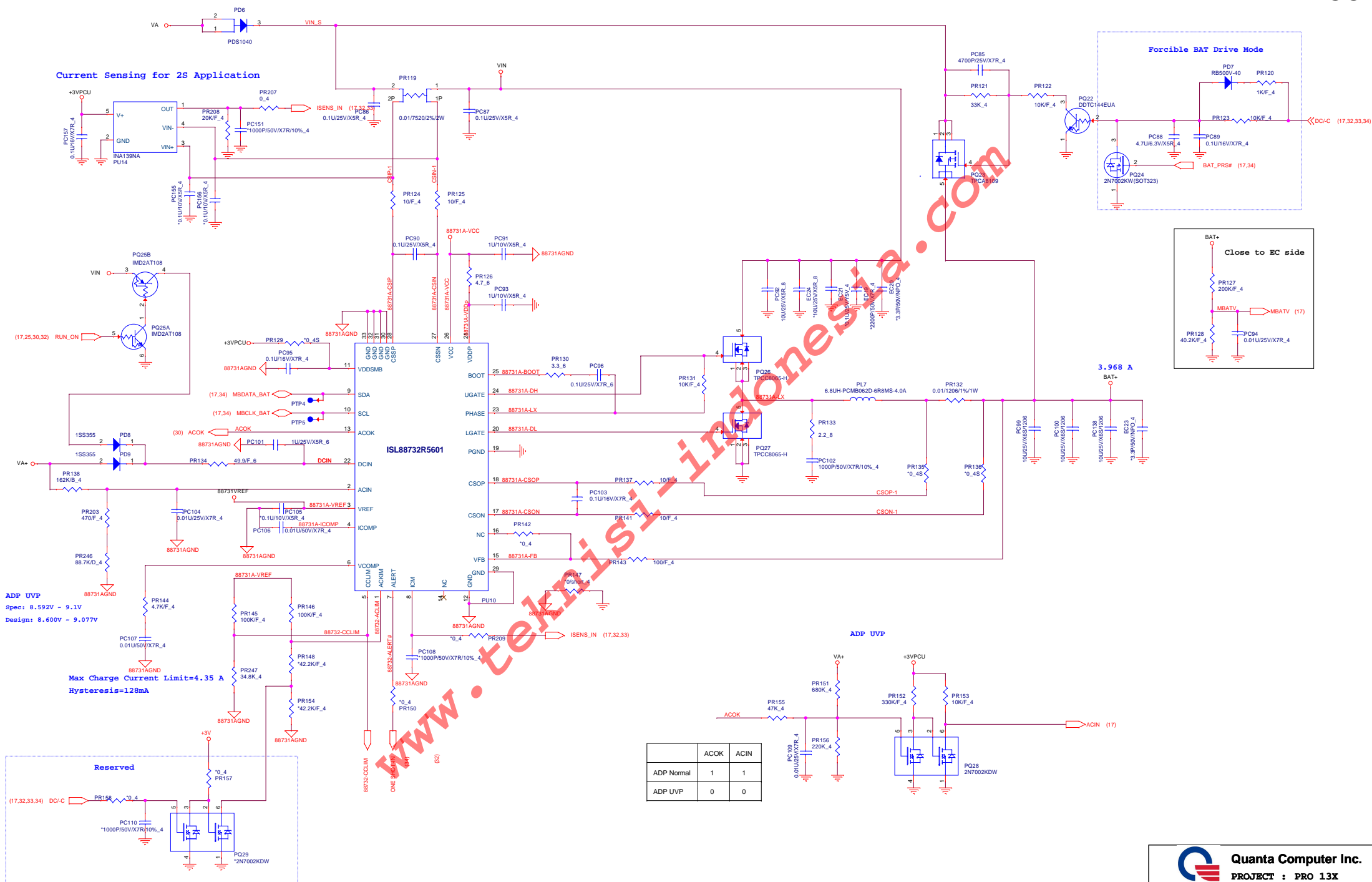


www.teknisi-indonesia.com



MB_DVT_026:PR113 & PR114 de-populate because of PWM IC has thermal protection

This part should not contain any substances which are specified in EM-S303.



HSW Power-Up Sequencing



SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BP935A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

Not support "DC only"

OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WLAN Enable	S4 (Win8 off) RTC wake Disable WLAN Disable	S5 Charge Enable	S5 Charge Disable Wol Disable	S5 Wol Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

PCI-E BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111G)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USB3.0
PORT 2	USB2.0
PORT 3	USB2.0
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	Card Reader
PORT 12	Touch Screen
PORT 13	N/A

This part should not contain any substances which are specified in EN-6303.

